

**CMOS Hex Voltage Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation**

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

CD4504BT Hex Voltage Level Shifter consists of six circuits which shift input signals from the V<sub>CC</sub> logic level to the V<sub>DD</sub> logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the V<sub>CC</sub> HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

**Specifications**

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the CD4504BT are contained in SMD 5962-96665. A "hot-link" is provided from our website for downloading.

[www.intersil.com/spacedefense/newsafclasst.asp](http://www.intersil.com/spacedefense/newsafclasst.asp)

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

[www.intersil.com/quality/manuals.asp](http://www.intersil.com/quality/manuals.asp)

**Ordering Information**

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9666501TEC	CD4504BDTR	-55 to 125
5962R9666501TXC	CD4504BKTR	-55 to 125

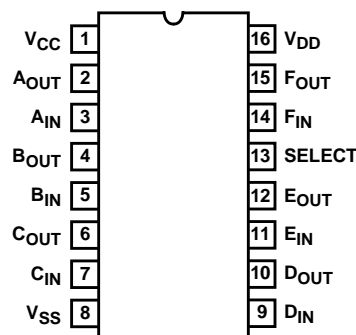
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

**Features**

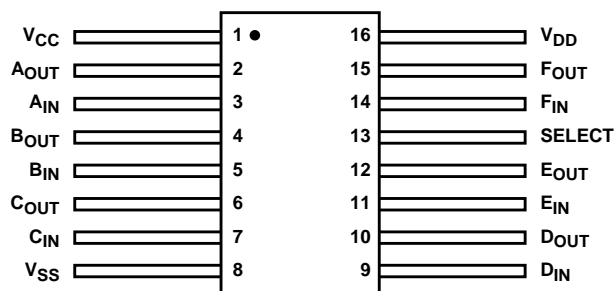
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10<sup>5</sup> RAD(Si)
  - SEP Effective LET > 75 MEV/gm/cm<sup>2</sup>
- Independence of Power Supply Sequence Considerations
  - V<sub>CC</sub> Can Exceed V<sub>DD</sub>
  - Input Signals can Exceed Both V<sub>CC</sub> and V<sub>DD</sub>
- Up and Down Level Shifting Capability
- Shiftable Input Threshold for Either CMOS or TTL Compatibility
- 100% Tested for Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics

**Pinouts**

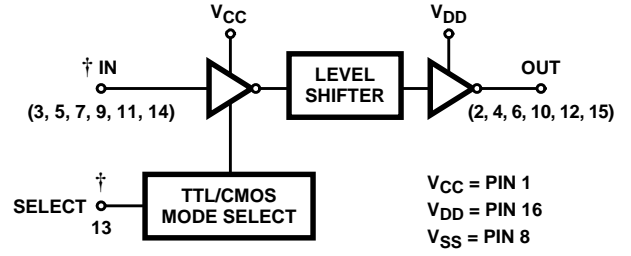
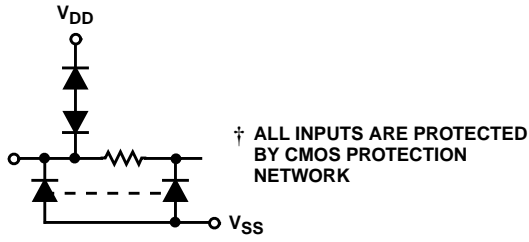
**CD4504BT (SBDIP), CDIP2-T16**  
TOP VIEW



**CD4504BT (FLATPACK), CDFP4-16**  
TOP VIEW



**Functional Diagram**



**Die Characteristics**

**DIE DIMENSIONS:**

(2540μm x 1753μm x 533μm ±25.4μm)  
 100 x 69 x 21mils ±1mil

**METALLIZATION:**

Type: Al  
 Thickness: 12.5kÅ ±1.5kÅ

**SUBSTRATE POTENTIAL:**

Leave Floating or Tie to V<sub>DD</sub>  
 Bond Pad #16 (V<sub>DD</sub>) First

**BACKSIDE FINISH:**

Silicon

**PASSIVATION:**

Type: Phosphorus Doped Silox (SiO<sub>2</sub>)  
 Thickness: 13.0kÅ ±2.6kÅ

**WORST CASE CURRENT DENSITY:**

< 2.0e5 A/cm<sup>2</sup>

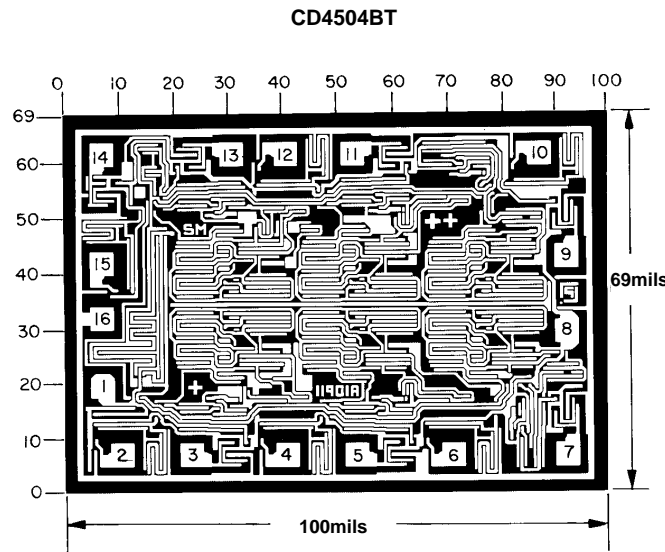
**TRANSISTOR COUNT:**

72

**PROCESS:**

Bulk CMOS

**Metallization Mask Layout**



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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