

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT646**

**Octal bus transceiver/register;  
3-state**

Product specification  
File under Integrated Circuits, IC06

September 1993

# Octal bus transceiver/register; 3-state

# 74HC/HCT646

## FEATURES

- Independent register for A and B buses
- Multiplexed real-time and stored data
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT646 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT646 consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the “A” or “B” bus will be

clocked into the registers as the appropriate clock (CP<sub>AB</sub> and CP<sub>BA</sub>) goes to a HIGH logic level. Output enable ( $\overline{OE}$ ) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the “A” or “B” register, or in both. The select source inputs (S<sub>AB</sub> and S<sub>BA</sub>) can multiplex stored and real-time (transparent mode) data. The direction (DIR) input determines which bus will receive data when  $\overline{OE}$  is active (LOW). In the isolation mode ( $\overline{OE} = \text{HIGH}$ ), “A” data may be stored in the “B” register and/or “B” data may be stored in the “A” register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The “646” is functionally identical to the “648”, but has non-inverting data paths.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	11	13	ns
f <sub>max</sub>	maximum clock frequency		69	85	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per channel	notes 1 and 2	30	33	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 f<sub>i</sub> = input frequency in MHz  
 f<sub>o</sub> = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in V
2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
 For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

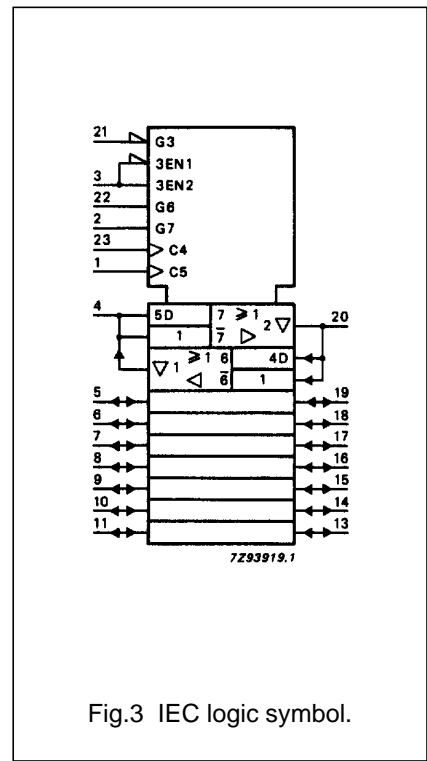
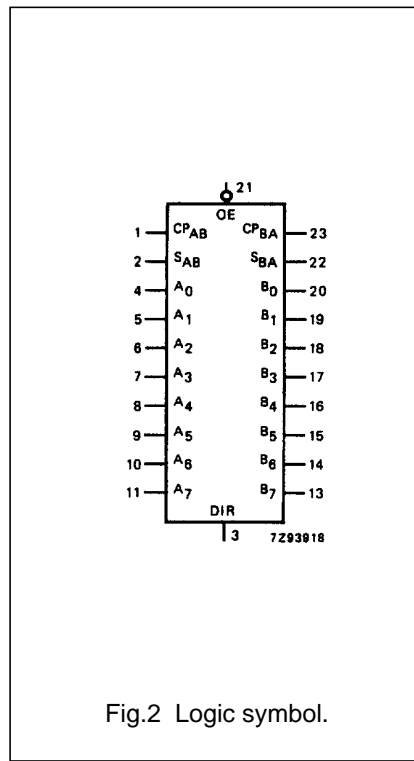
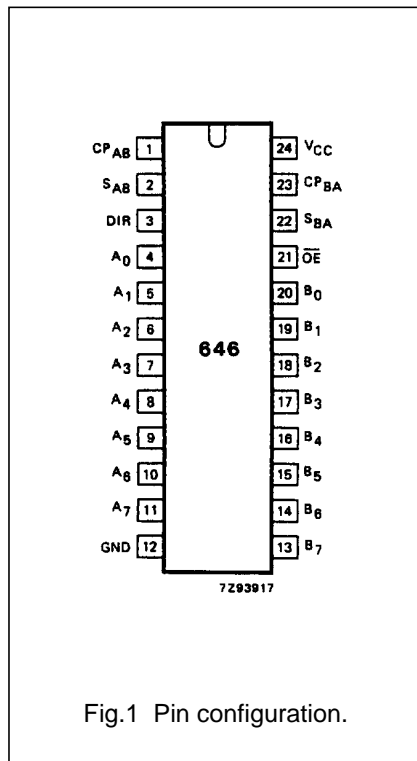
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

Octal bus transceiver/register; 3-state

74HC/HCT646

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	CP <sub>AB</sub>	A to B clock input (LOW-to-HIGH, edge-triggered)
2	S <sub>AB</sub>	select A to B source input
3	DIR	direction control input
4, 5, 6, 7, 8, 9, 10, 11	A <sub>0</sub> to A <sub>7</sub>	A data inputs/outputs
12	GND	ground (0 V)
20, 19, 18, 17, 16, 15, 14, 13	B <sub>0</sub> to B <sub>7</sub>	B data inputs/outputs
21	$\overline{OE}$	output enable input (active LOW)
22	S <sub>BA</sub>	select B to A source input
23	CP <sub>BA</sub>	B to A clock input (LOW-to-HIGH, edge-triggered)
24	V <sub>CC</sub>	positive supply voltage



Octal bus transceiver/register; 3-state

74HC/HCT646

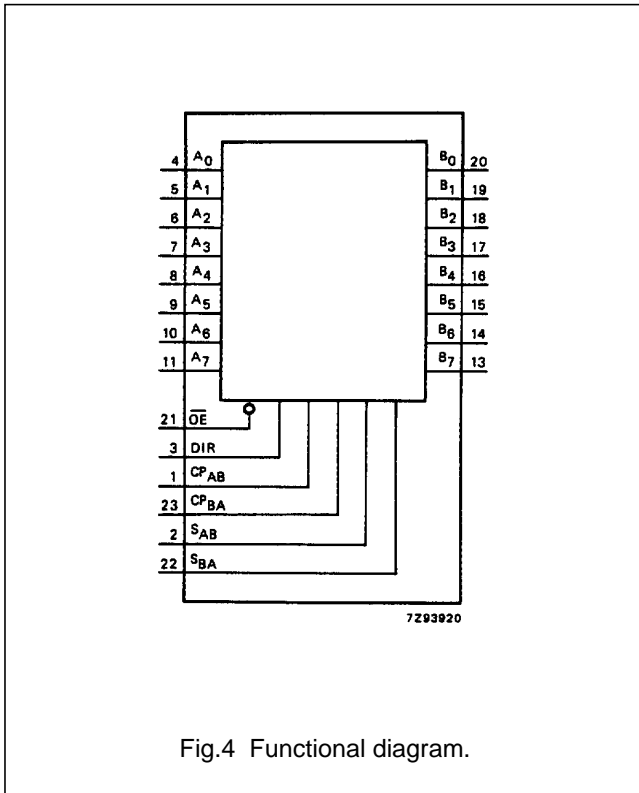


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS (1)						DATA I/O (2)		FUNCTION
OE	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>	A <sub>0</sub> to A <sub>7</sub>	B <sub>0</sub> to B <sub>7</sub>	
H	X	H or L	H or L	X	X	input	input	isolation
H	X	↑	↑	X	X	input	input	store A and B data
L	L	X	X	X	L	output	input	real-time B data to A bus
L	L	X	H or L	X	H	output	input	stored B data to A bus
L	H	X	X	L	X	input	output	real-time A data to B bus
L	H	H or L	X	H	X	input	output	stored A data to B bus

Notes

- H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH level transition
- The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

Octal bus transceiver/register; 3-state

74HC/HCT646

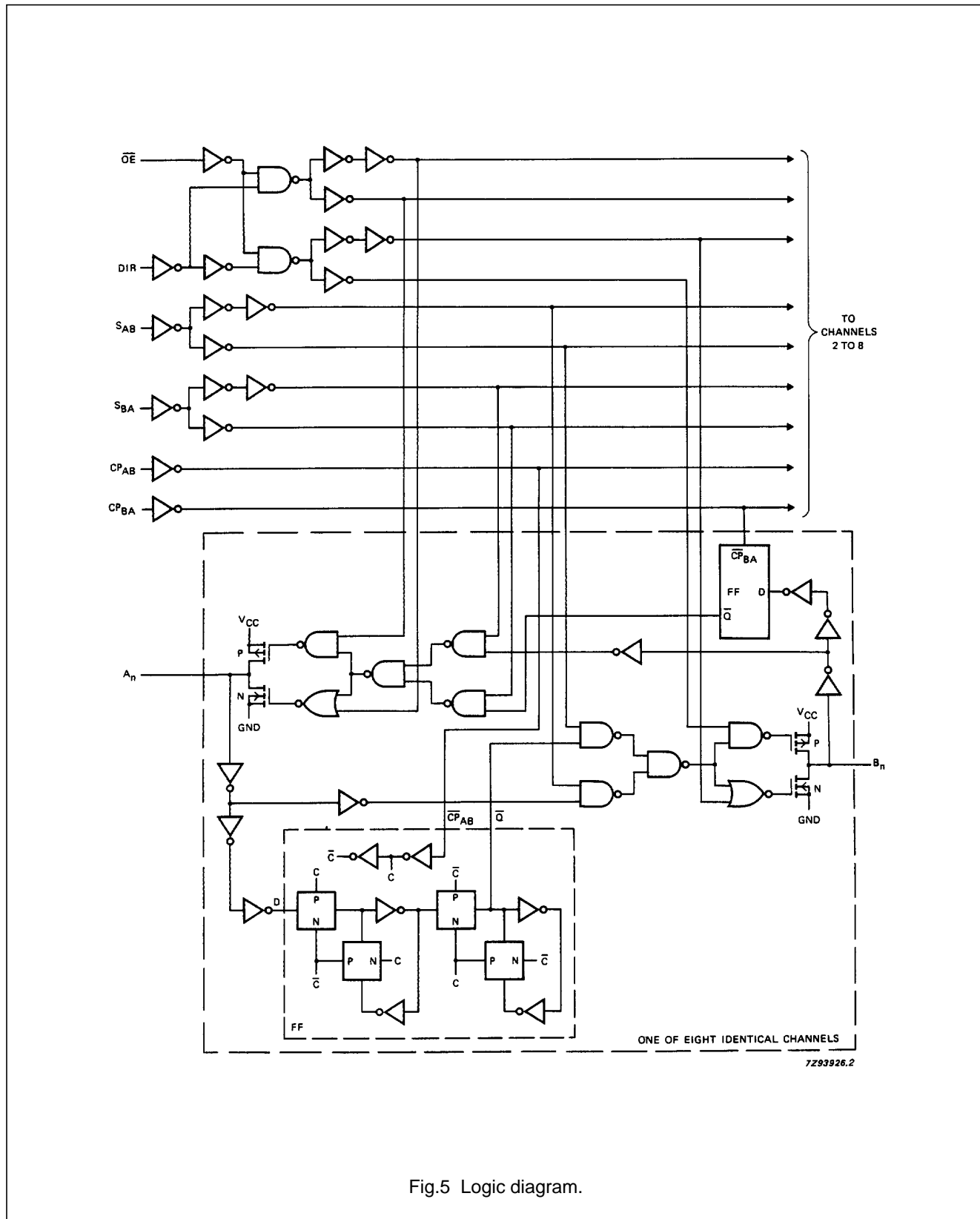


Fig.5 Logic diagram.

## Octal bus transceiver/register; 3-state

## 74HC/HCT646

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> ,B <sub>n</sub> to B <sub>n</sub> ,A <sub>n</sub>		39 14 11	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>AB</sub> ,CP <sub>BA</sub> to B <sub>n</sub> ,A <sub>n</sub>		66 24 19	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>AB</sub> ,S <sub>BA</sub> to B <sub>n</sub> ,A <sub>n</sub>		55 20 16	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.8
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{\text{OE}}$ to A <sub>n</sub> ,B <sub>n</sub>		47 17 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.9
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{\text{OE}}$ to A <sub>n</sub> ,B <sub>n</sub>		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.9
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time DIR to A <sub>n</sub> ,B <sub>n</sub>		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.10
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time DIR to A <sub>n</sub> ,B <sub>n</sub>		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.10
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6 and Fig.8
t <sub>W</sub>	clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	80 16 14	25 9 7		100 24 20		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>SU</sub>	set-up time A <sub>n</sub> ,B <sub>n</sub> to CP <sub>AB</sub> ,CP <sub>BA</sub>	60 12 10	-3 -1 -1		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t <sub>H</sub>	hold time A <sub>n</sub> ,B <sub>n</sub> to CP <sub>AB</sub> ,CP <sub>BA</sub>	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig.7
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	21 63 75		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

## Octal bus transceiver/register; 3-state

74HC/HCT646

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
S <sub>AB</sub> , S <sub>BA</sub>	0.60
A <sub>0</sub> to A <sub>7</sub> and B <sub>0</sub> to B <sub>7</sub>	0.75

INPUT	UNIT LOAD COEFFICIENT
CP <sub>AB</sub> , CP <sub>BA</sub>	1.50
$\overline{OE}$	1.50
DIR	1.25

## Octal bus transceiver/register; 3-state

## 74HC/HCT646

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

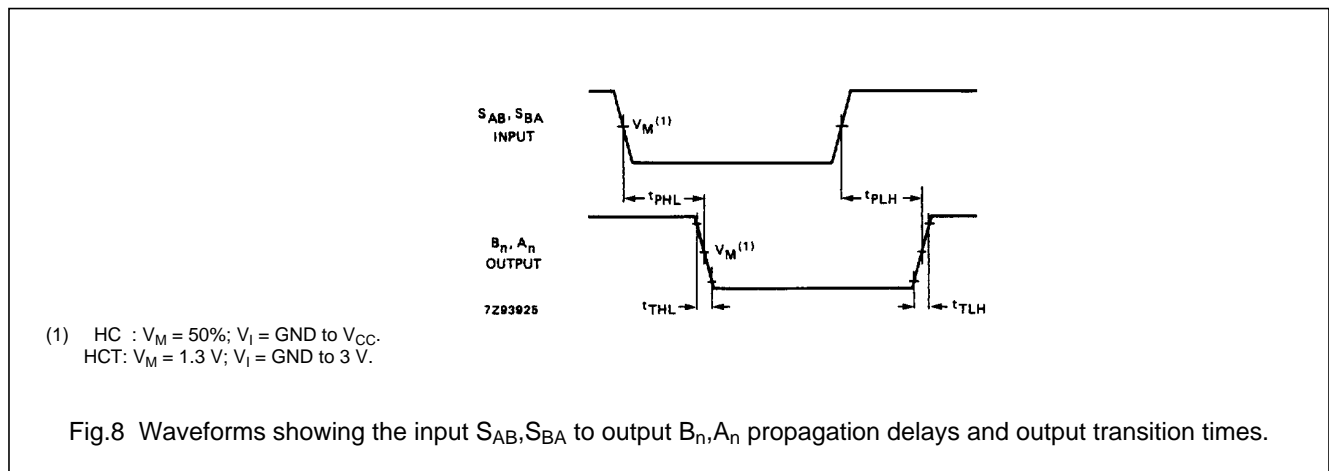
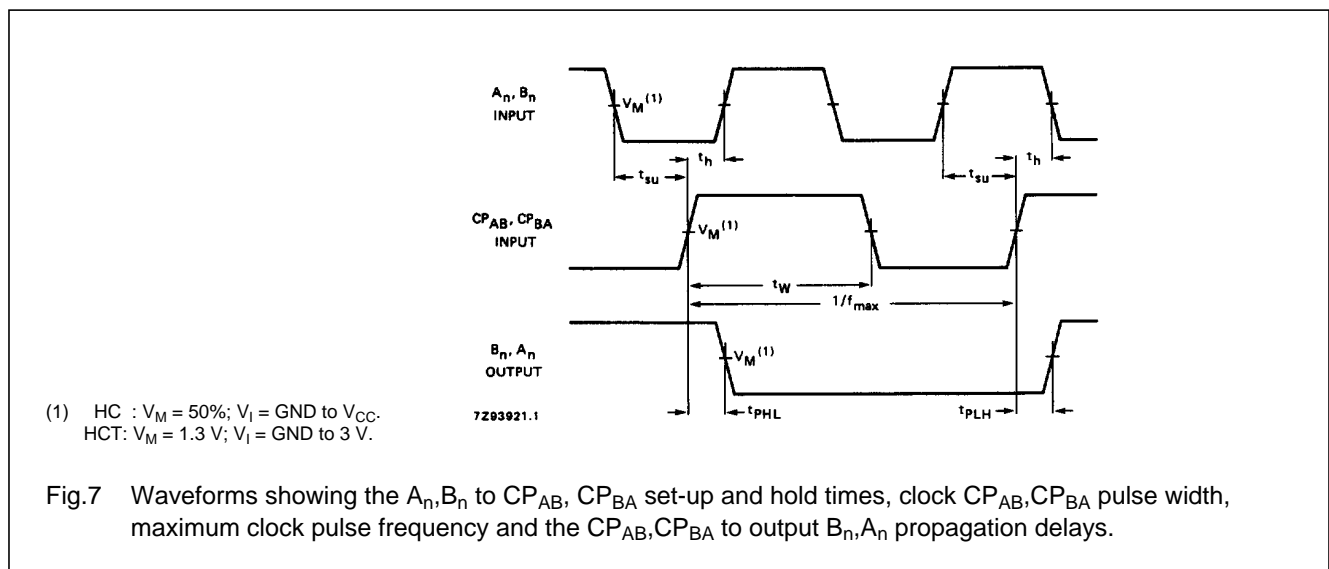
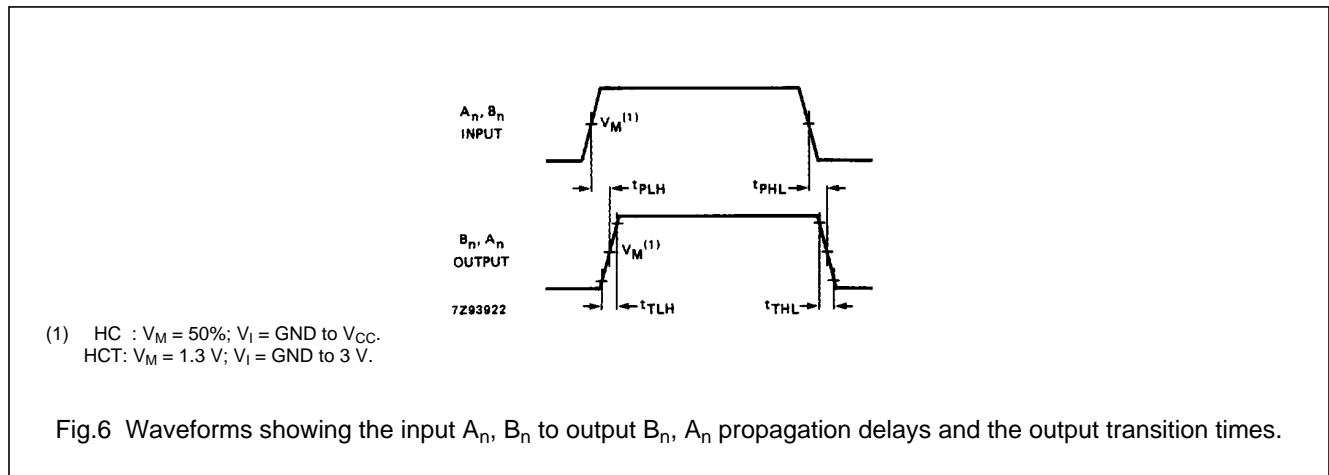
SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HCT									V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> ,B <sub>n</sub> to B <sub>n</sub> ,A <sub>n</sub>		16	30		38		45	ns	4.5	Fig.6	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP <sub>AB</sub> ,CP <sub>BA</sub> to B <sub>n</sub> ,A <sub>n</sub>		23	44		55		66	ns	4.5	Fig.7	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay S <sub>AB</sub> ,S <sub>BA</sub> to B <sub>n</sub> ,A <sub>n</sub>		26	46		58		69	ns	4.5	Fig.8	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to A <sub>n</sub> ,B <sub>n</sub>		21	40		50		60	ns	4.5	Fig.9	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to A <sub>n</sub> ,B <sub>n</sub>		20	35		44		53	ns	4.5	Fig.9	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time DIR to A <sub>n</sub> ,B <sub>n</sub>		21	40		50		60	ns	4.5	Fig.10	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time DIR to A <sub>n</sub> ,B <sub>n</sub>		21	35		44		53	ns	4.5	Fig.10	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6 and Fig.8	
t <sub>w</sub>	clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	16	8		20		24		ns	4.5	Fig.7	
t <sub>su</sub>	set-up time A <sub>n</sub> ,B <sub>n</sub> to CP <sub>AB</sub> ,CP <sub>BA</sub>	12	3		15		18		ns	4.5	Fig.7	
t <sub>h</sub>	hold time A <sub>n</sub> ,B <sub>n</sub> to CP <sub>AB</sub> ,CP <sub>BA</sub>	5	1		5		5		ns	4.5	Fig.7	
f <sub>max</sub>	maximum clock pulse frequency	30	77		24		20		MHz	4.5	Fig.7	



Octal bus transceiver/register; 3-state

74HC/HCT646

AC WAVEFORMS



Octal bus transceiver/register; 3-state

74HC/HCT646

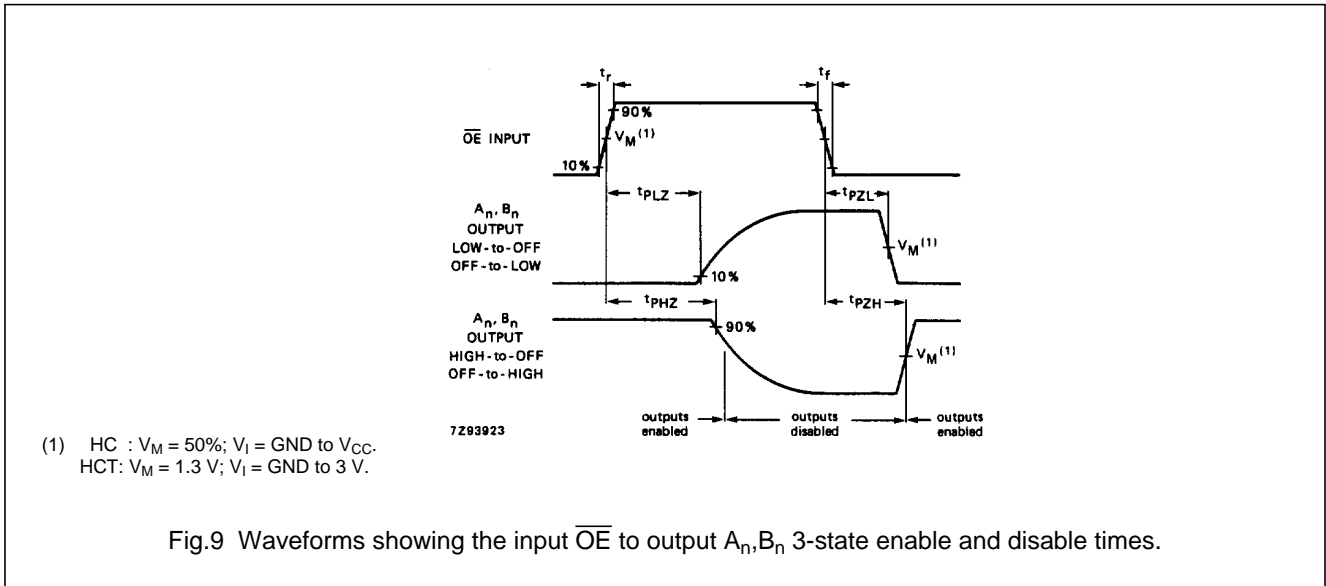


Fig.9 Waveforms showing the input  $\overline{\text{OE}}$  to output  $A_n, B_n$  3-state enable and disable times.

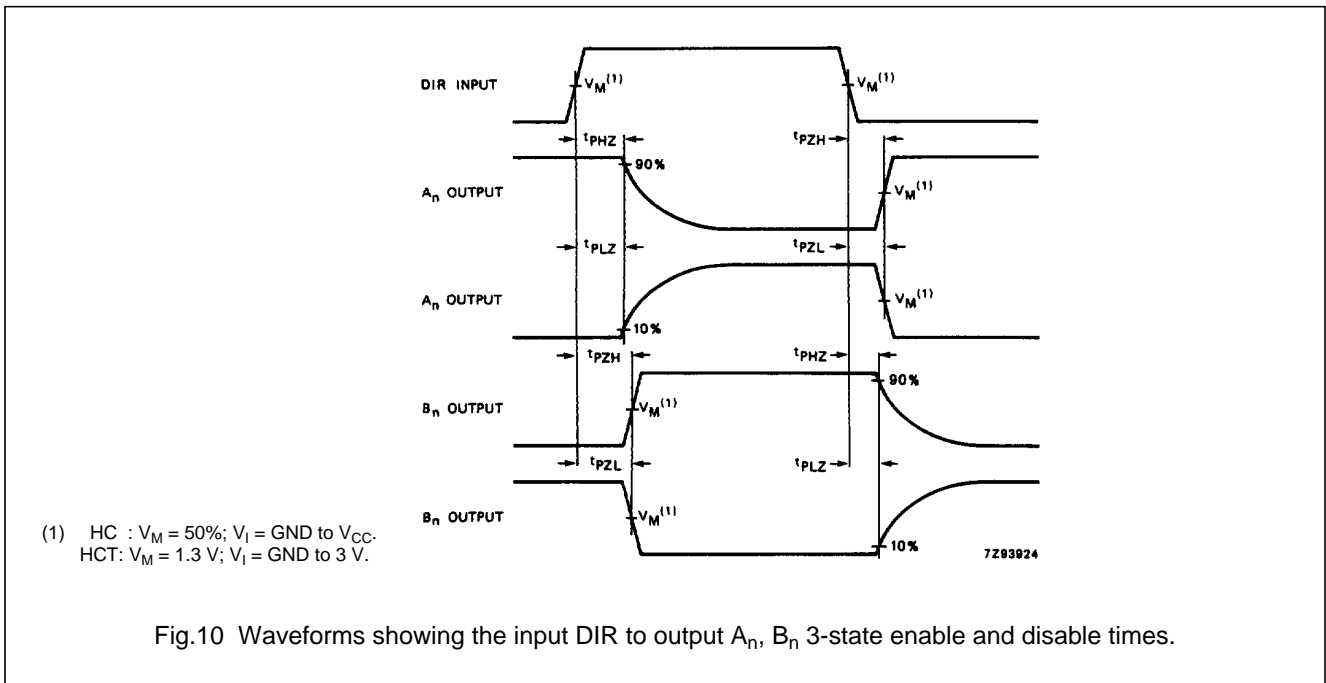


Fig.10 Waveforms showing the input DIR to output  $A_n, B_n$  3-state enable and disable times.

Octal bus transceiver/register; 3-state

74HC/HCT646

APPLICATION INFORMATION

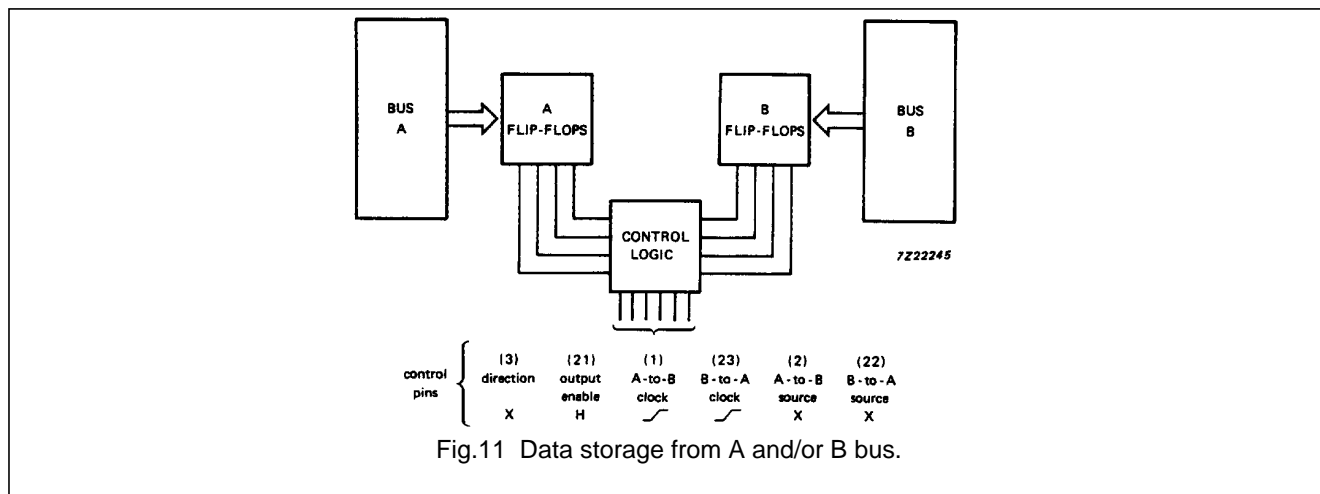


Fig.11 Data storage from A and/or B bus.

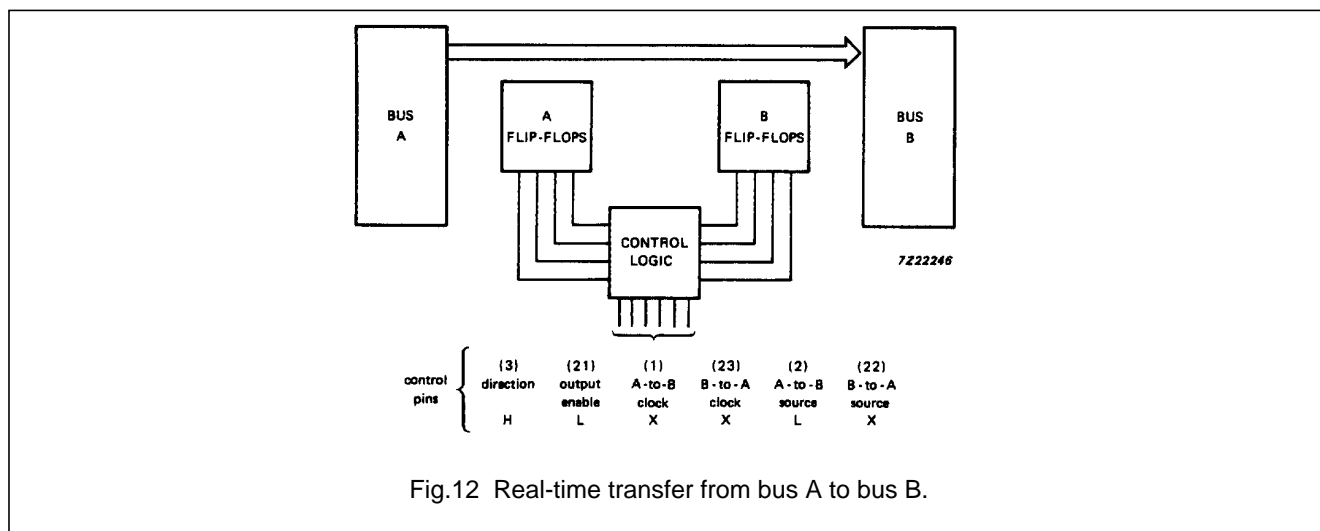


Fig.12 Real-time transfer from bus A to bus B.

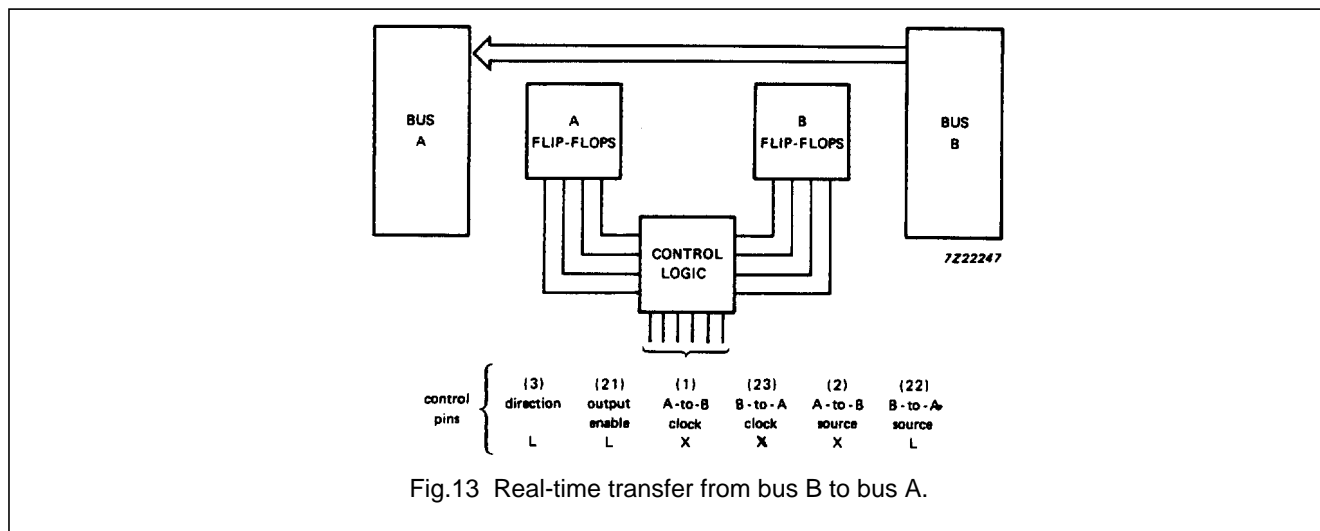


Fig.13 Real-time transfer from bus B to bus A.

Octal bus transceiver/register; 3-state

74HC/HCT646

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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.