

8-Bit Bus Register Transceivers and Latch Transceivers

SN54/74LS546 SN54/74LS547 SN54/74LS566 SN54/74LS567

Features/Benefits

- Bidirectional transceivers utilizing registers or latches
- Faster than other LS-TTL registers/latches
- Independent registers/latches for A bus and B bus
- Data can be swapped between internal registers/latches
- 8-bit data paths match byte boundaries
- 'LS546/547/566/567 can replace two 'LS374/373/534/533 devices
- Independent clock/gate enables for rank A and rank B
- High drive capability: $I_{OL} = 32 \text{ mA (COM)}, 24 \text{ mA (MIL)}$
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- The clock, clock-enable, and latch-enable inputs typically have 300 mV hysteresis

There are independent clock and clock enable controls for the two directions namely CKA, CKB, CKEA, CKEB for 'LS546/'LS566, and independent gate enable control GA1, GA2, GB1 and GB2 for 'LS547/'LS567. The CKA/B and CKEA/B can control the internal registers A/B to load data or hold data. Similarly, the GA1, GA2, GB1 and GB2 can govern the internal latches, A/B to pass or hold data.

Description

These devices are comprised of a pair of 8-bit registers ('LS546, 'LS566), or a pair of 8-bit latches ('LS547, 'LS567).

The direction of operation is controlled by \overline{OEAB} and \overline{OEBA} . When \overline{OEAB} is Low and \overline{OEBA} is High, the operation of the registers/latches is A-to-B direction; when \overline{OEAB} is High and \overline{OEBA} is low, the operation of the registers/latches is B-to-A direction; when \overline{OEAB} and \overline{OEBA} both are High, the A, B buses both are inputs, data will be stored into registers/latches; when \overline{OEAB} and \overline{OEBA} both are Low, the A, B buses both are outputs, data will transfer from internal registers/latches to A, B buses.

There are independent clock and clock enable controls for the two directions: namely CKA, CKB, CKEA and CKEB for 'LS546/'LS566, and independent gate enable control GA1, GA2, GB1 and GB2 for 'LS547/'LS567. The CKA/B and CKEA/B can control the internal registers A/B to load data or hold data. Similarly, the GA1, GA2, GB1 and GB2 govern the internal latches, A/B to pass or hold data.

The 'LS546/'547 provide non-inverting polarity; the 'LS566/'LS567 provide inverting polarity. The 'LS546/'LS547/'LS566/'LS567 all have 3-state outputs, and have 32-mA output drive I_{OL} (COM) over the commercial temperature range and 24-mA output drive I_{OL} (MIL), over the military temperature range.

All of the devices are packaged in the popular 24-pin SKINNYDIP package.

Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE | POLARITY | TYPE | POWER | |
|-------------|-----------------|-------------|------------|----------|-------|----------|
| SN54LS546 | JS, W, L (28) | Mil | Non-invert | Register | LS | |
| SN74LS546 | NS, JS, NL (28) | Com | | Latch | | |
| SN54LS547 | JS, W, L (28) | Mil | | Invert | | Register |
| SN74LS547 | NS, JS, NL (28) | Com | | | | Latch |
| SN54LS566 | JS, W, L (28) | Mil | Invert | | | Register |
| SN74LS566 | NS, JS, NL (28) | Com | | | | Latch |
| SN54LS567 | JS, W, L (28) | Mil | | Invert | | Register |
| SN74LS567 | NS, JS, NL (28) | Com | | | | Latch |

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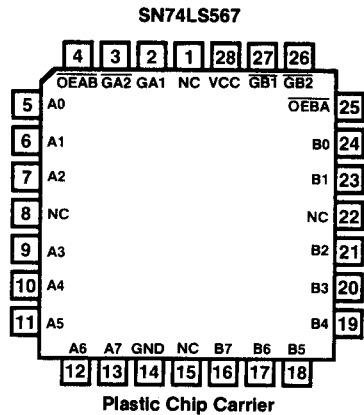
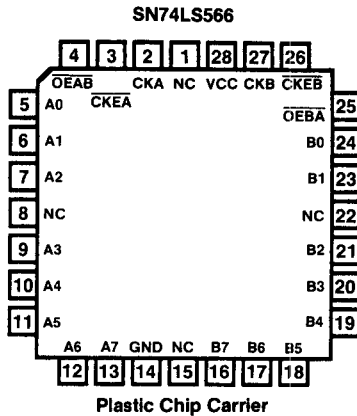
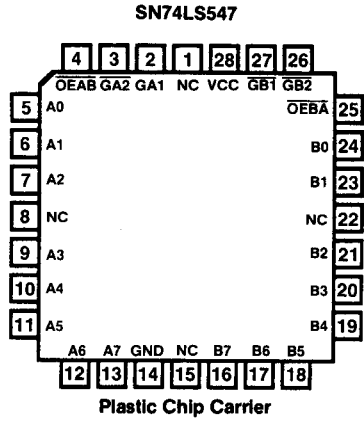
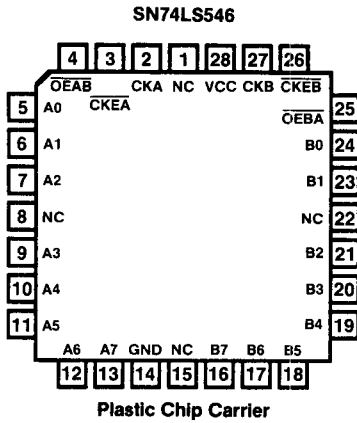
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

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TWX: 910-338-2376

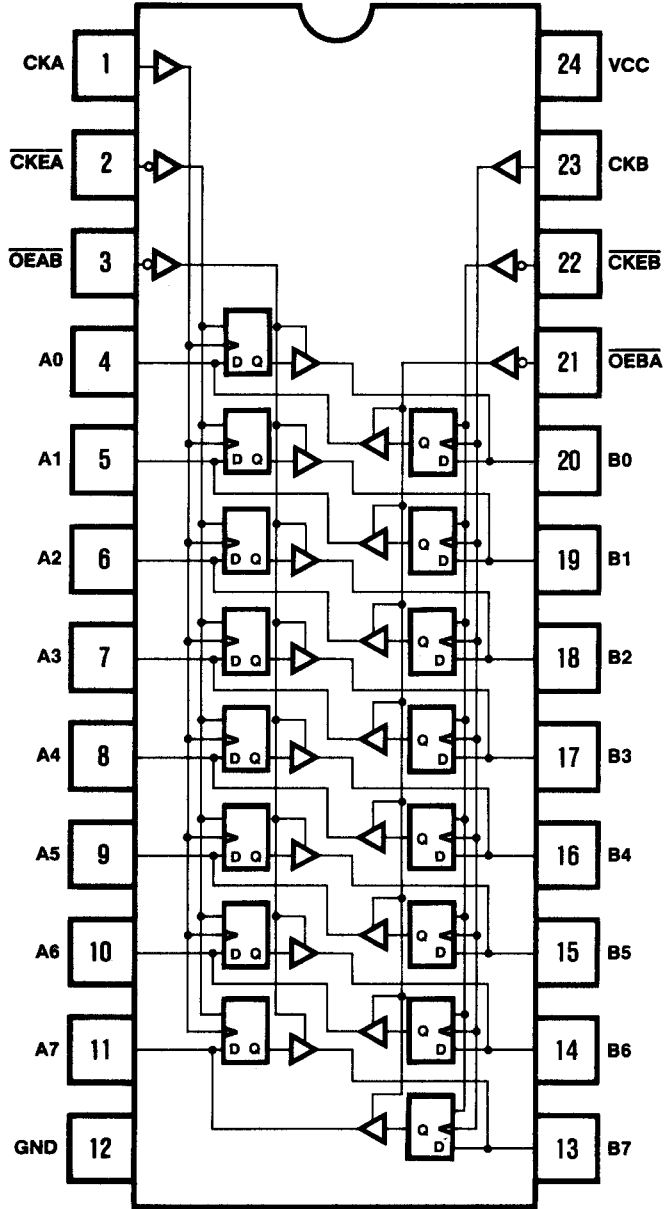
**Monolithic
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Pin Configurations



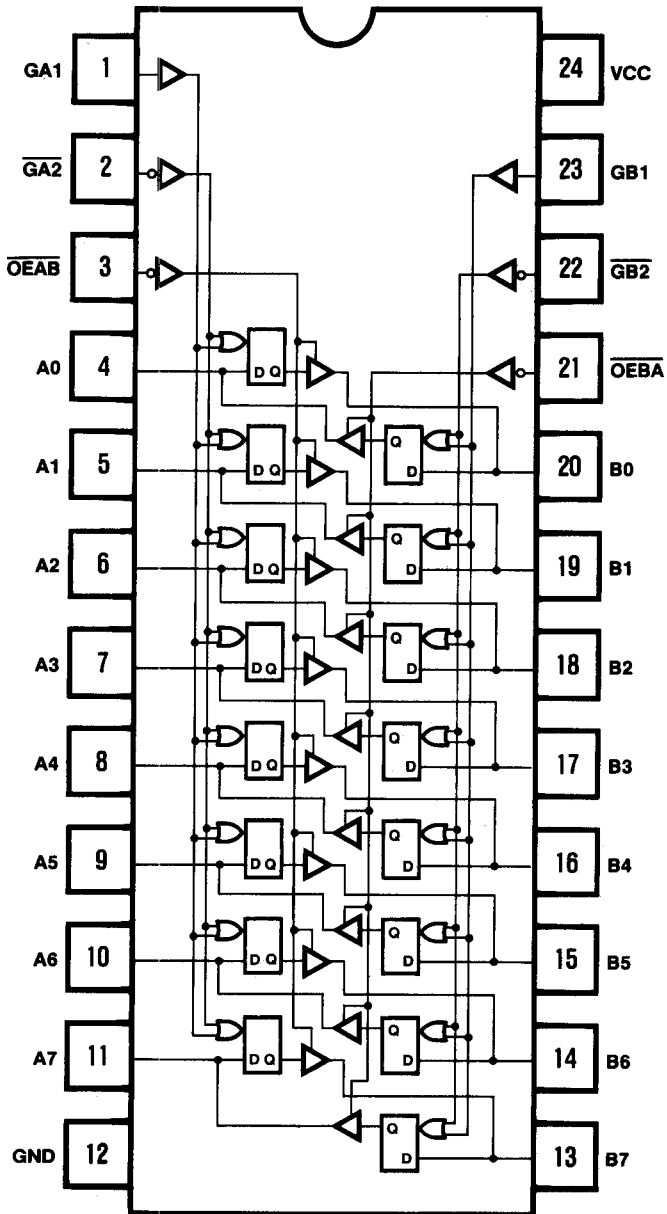
Logic Diagram

SN54/74LS546
REGISTER TRANSCEIVER
NON-INVERTING OUTPUTS



Logic Diagram

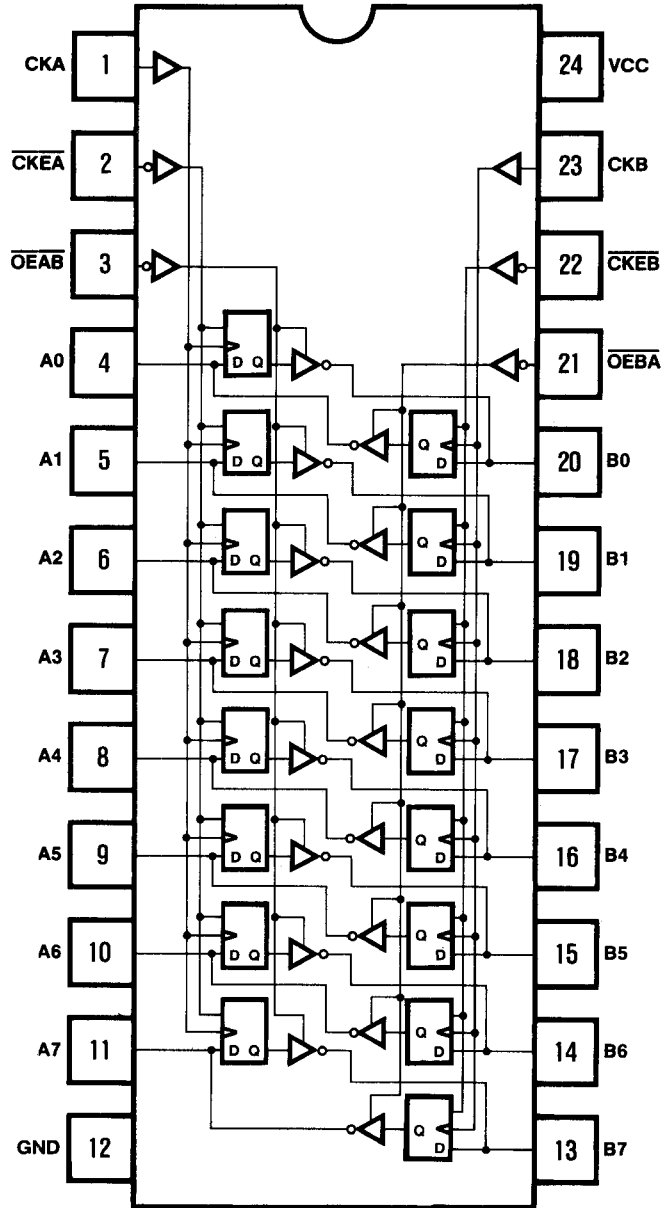
SN54/74LS547
LATCH TRANSCEIVER
NON-INVERTING OUTPUTS



13

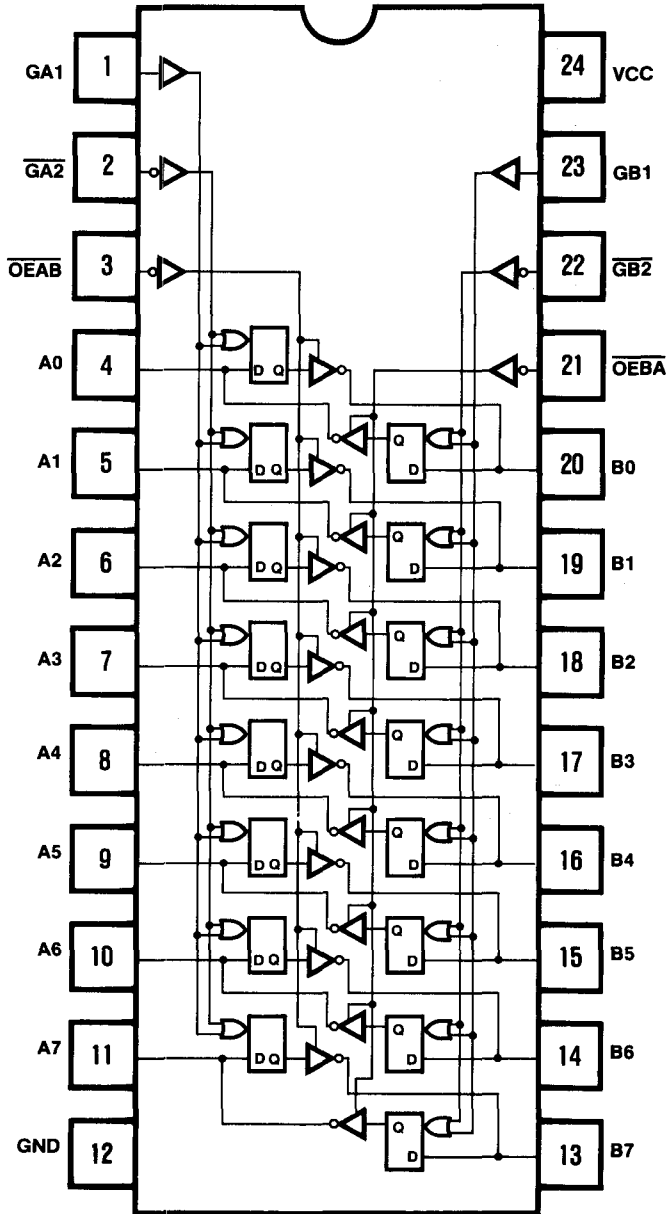
Logic Diagram

SN54/74LS566
REGISTER TRANSCEIVER
INVERTING OUTPUTS



Logic Diagram

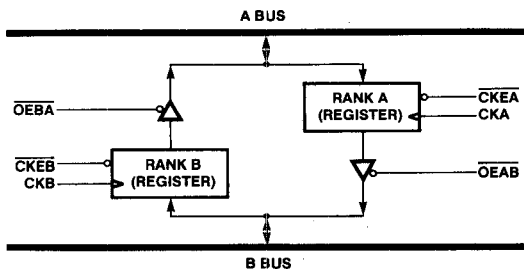
SN54/74LS567
LATCH TRANSCEIVER
INVERTING OUTPUTS



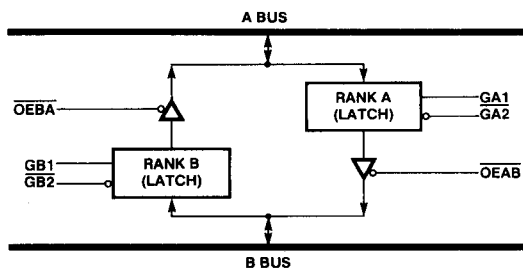
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Block Diagrams

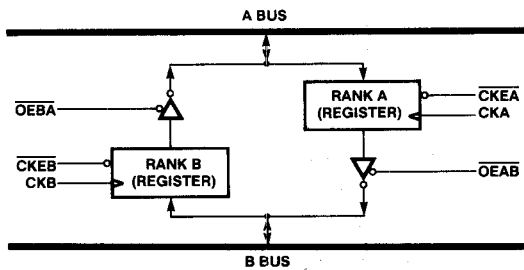
'LS546 (Non-Inverting)



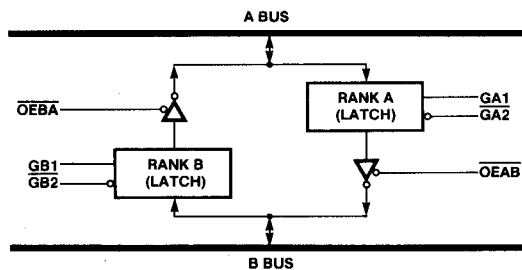
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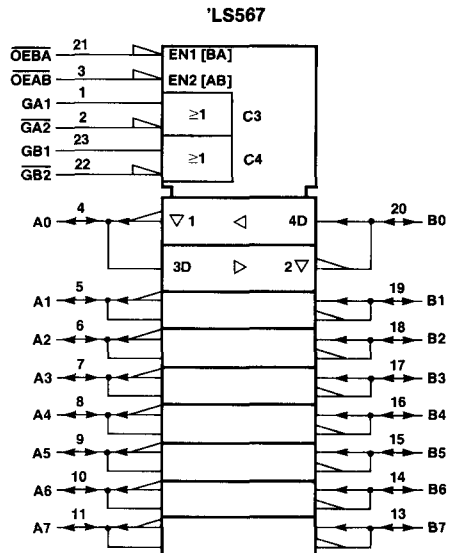
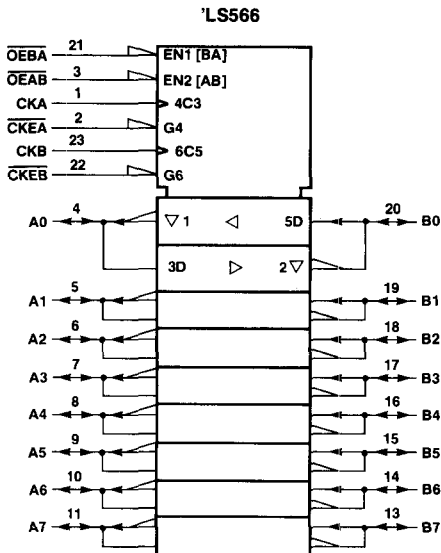
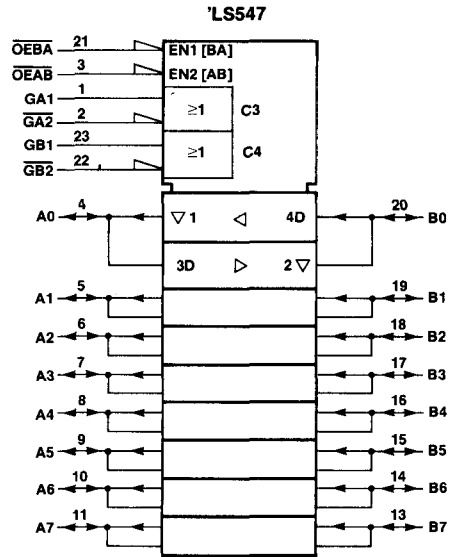
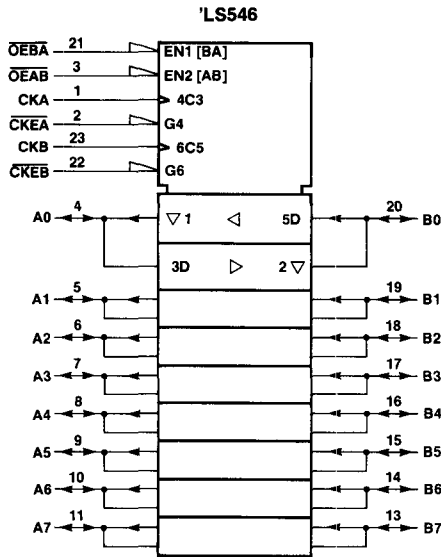
'LS566 (Inverting)



'LS567 (Inverting)



IEEE Symbols



Function Table
Nomenclature Description

A0-A7: Eight input/output pins on the A side.
B0-B7: Eight input/output pins on the B side.
X: H or L state irrelevant ("Don't Care" conditions).

GA1/GA2: Gate enables for rank A of 'LS547/'LS567.
GB1/GB2: Gate enables for rank B of 'LS547/'LS567.
QoA/QoB: Previous data of the internal rank A/B.

| GA1 | GA2 | RANK A | GB1 | GB2 | RANK B |
|-----|-----|-------------------|-----|-----|-------------------|
| X | L | Enabled (Flush) | X | L | Enabled (Flush) |
| X | L | Enabled (Flush) | L | H | Disabled (Freeze) |
| X | L | Enabled (Flush) | H | X | Enabled (Flush) |
| L | H | Disabled (Freeze) | H | X | Enabled (Flush) |
| L | H | Disabled (Freeze) | X | L | Enabled (Flush) |
| L | H | Disabled (Freeze) | L | H | Disabled (Freeze) |
| H | X | Enabled (Flush) | X | L | Enabled (Flush) |
| H | X | Enabled (Flush) | L | H | Disabled (Freeze) |
| H | X | Enabled (Flush) | H | X | Enabled (Flush) |

CKEA/CKEB: Clock enable for rank A/B of 'LS546/'LS566.

CKA/CKB: Clock for rank A/B of 'LS546/'LS566.

UC: H or L or \uparrow case (nonclocked operation).

†: Positive edge of CK causes clocking, if clock enable is asserted.

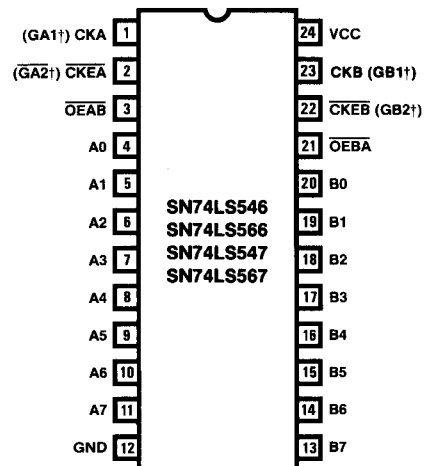
| CKA | CKEA | RANK A | CKB | CKEB | RANK B |
|------------|------|----------|------------|------|----------|
| UC | X | Disabled | UC | X | Disabled |
| \uparrow | L | Enabled | \uparrow | L | Enabled |
| \uparrow | L | Enabled | \uparrow | H | Disabled |
| \uparrow | H | Disabled | \uparrow | L | Enabled |
| \uparrow | H | Disabled | \uparrow | H | Disabled |

OEAB: To enable the A-to-B operation.

OEBA: To enable the B-to-A operation.

| OEAB | OEBA | OPERATION DIRECTION |
|------|------|--|
| L | L | A, B buses both are outputs (Transfer stored data to bus stored) |
| L | H | A-to-B |
| H | L | B-to-A |
| H | H | A, B buses both are inputs (storage) |

Pin Configuration



† For SN74LS547, SN74LS567

Bus Operation For 'LS546

| OPERATION | DIRECTION CONTROL | | DATA I/O | | BLOCK DIAGRAM | CLOCK ENABLE (A) | | RANK A | CLOCK ENABLE (B) | | RANK B |
|----------------------|-------------------|------|------------------|------------------|---------------|------------------|------|--------|------------------|------|--------|
| | OEAB | OEBA | A0-A7 | B0-B7 | | CKA | CKEA | | CKB | CKEB | |
| | | | | | | | | | | | |
| Storage | H | H | Input | Input | | UC | X | QoA | UC | X | QoB |
| | | | | | | UC | X | QoA | ↑ | L | B bus |
| | | | | | | UC | X | QoA | ↑ | H | QoB |
| | | | | | | ↑ | L | A bus | UC | X | QoB |
| | | | | | | ↑ | L | A bus | ↑ | L | B bus |
| | | | | | | ↑ | L | A bus | ↑ | H | QoB |
| | | | | | | ↑ | H | QoA | UC | X | QoB |
| | | | | | | ↑ | H | QoA | ↑ | H | QoB |
| B-to-A Operation | H | L | Output of Rank B | Input | | UC | X | QoA | UC | X | QoB |
| | | | | | | UC | X | QoA | ↑ | L | B bus |
| | | | | | | UC | X | QoA | ↑ | H | QoB |
| | | | | | | ↑ | L | Rank B | UC | X | QoB |
| | | | | | | ↑ | L | Rank B | ↑ | L | B bus |
| | | | | | | ↑ | L | Rank B | ↑ | H | QoB |
| | | | | | | ↑ | H | QoA | UC | X | QoB |
| | | | | | | ↑ | H | QoA | ↑ | L | B bus |
| A-to-B Operation | L | H | Input | Output of Rank A | | UC | X | QoA | UC | X | QoB |
| | | | | | | UC | X | QoA | ↑ | L | Rank A |
| | | | | | | UC | X | QoA | ↑ | H | QoB |
| | | | | | | ↑ | L | A bus | UC | X | QoB |
| | | | | | | ↑ | L | A bus | ↑ | L | Rank A |
| | | | | | | ↑ | L | A bus | ↑ | H | QoB |
| | | | | | | ↑ | H | QoA | UC | X | QoB |
| | | | | | | ↑ | H | QoA | ↑ | L | Rank A |
| Transfer Stored Data | L | L | Output of Rank B | Output of Rank A | | UC | X | QoA | UC | X | QoB |
| | | | | | | UC | X | QoA | ↑ | L | Rank A |
| | | | | | | UC | X | QoA | ↑ | H | QoB |
| | | | | | | ↑ | L | Rank B | UC | X | QoB |
| | | | | | | ↑ | L | Rank B | ↑ | L | Rank A |
| | | | | | | ↑ | L | Rank B | ↑ | H | QoB |
| | | | | | | ↑ | H | QoA | UC | X | QoB |
| | | | | | | ↑ | H | QoA | ↑ | L | Rank A |
| ↑ | H | QoA | ↑ | H | QoB | | | | | | |

Bus Operation For 'LS547

| OPERATION | DIRECTION CONTROL | | DATA I/O | | BLOCK DIAGRAM | GATE ENABLE (A) | | RANK A | GATE ENABLE (B) | | RANK B |
|----------------------|-------------------|------|------------------|------------------|---------------|-----------------|-----|--------|-----------------|-----|--------|
| | OEAB | OEBA | A0-A7 | B0-B7 | | GA1 | GA2 | | GB1 | GB2 | |
| | Storage | H | H | Input | | Input | | L | H | QoA | L |
| L | | | | | H | | | QoA | H | X | B bus |
| L | | | | | H | | | QoA | X | L | B bus |
| H | | | | | X | | | A bus | L | H | QoB |
| H | | | | | X | | | A bus | H | X | B bus |
| H | | | | | X | | | A bus | X | L | B bus |
| X | | | | | L | | | A bus | L | H | QoB |
| X | | | | | L | | | A bus | H | X | B bus |
| X | | | | | L | | | A bus | X | L | B bus |
| B-to-A Operation | H | L | Output of Rank B | Input | | L | H | QoA | L | H | QoB |
| | | | | | | L | H | QoA | H | X | B bus |
| | | | | | | L | H | QoA | X | L | B bus |
| | | | | | | H | X | Rank B | L | H | QoB |
| | | | | | | H | X | Rank B | H | X | B bus |
| | | | | | | H | X | Rank B | X | L | B bus |
| | | | | | | X | L | Rank B | L | H | QoB |
| | | | | | | X | L | Rank B | H | X | B bus |
| | | | | | | X | L | Rank B | X | L | B bus |
| A-to-B Operation | L | H | Input | Output of Rank A | | L | H | QoA | L | H | QoB |
| | | | | | | L | H | QoA | H | X | Rank A |
| | | | | | | L | H | QoA | X | L | Rank A |
| | | | | | | H | X | A bus | L | H | QoB |
| | | | | | | H | X | A bus | H | X | Rank A |
| | | | | | | H | X | A bus | X | L | Rank A |
| | | | | | | X | L | A bus | L | H | QoB |
| | | | | | | X | L | A bus | H | X | Rank A |
| | | | | | | X | L | A bus | X | L | Rank A |
| Transfer Stored Data | L | L | Output of Rank B | Output of Rank A | | L | H | QoA | L | H | QoB |
| | | | | | | L | H | QoA | H | X | Rank A |
| | | | | | | L | H | QoA | X | L | Rank A |
| | | | | | | H | X | Rank B | L | H | QoB |
| | | | | | | H* | X | Rank B | H | X | Rank A |
| | | | | | | H* | X | Rank B | X | L | Rank A |
| | | | | | | X | L | Rank B | L | H | QoB |
| | | | | | | X* | L | Rank B | H | X | Rank A |
| | | | | | | X* | L | Rank B | X | L | Rank A |

* NOTE: These controls for OEAB, OEBA, GA1, GA2, GB1 and GB2 can cause race conditions.

Bus Operation For 'LS566

| OPERATION | DIRECTION CONTROL | | DATA I/O | | BLOCK DIAGRAM | CLOCK ENABLE (A) | | RANK A | CLOCK ENABLE (B) | | RANK B |
|----------------------|-------------------|-------------------|------------------|------------------|---------------|------------------|-------------------|--------|------------------|-------------------|--------|
| | \overline{OEAB} | \overline{OEBA} | A0-A7 | B0-B7 | | CKA | \overline{CKEA} | | CKB | \overline{CKEB} | |
| | Storage | H | H | Input | | Input | | | UC | X | |
| UC | | | | | X | | | QoA | ↑ | L | B bus |
| UC | | | | | X | | | QoA | ↑ | H | QoB |
| ↑ | | | | | L | | | A bus | UC | X | QoB |
| ↑ | | | | | L | | | A bus | ↑ | L | B bus |
| ↑ | | | | | L | | | A bus | ↑ | H | QoB |
| ↑ | | | | | H | | | QoA | UC | X | QoB |
| ↑ | | | | | H | | | QoA | ↑ | L | B bus |
| ↑ | | | | | H | | | QoA | ↑ | H | QoB |
| B-to-A Operation | H | L | Output of Rank B | Input | | UC | X | QoA | UC | X | QoB |
| | | | | | | UC | X | QoA | ↑ | L | B bus |
| | | | | | | UC | X | QoA | ↑ | H | QoB |
| | | | | | | ↑ | L | Rank B | UC | X | QoB |
| | | | | | | ↑ | L | Rank B | ↑ | L | B bus |
| | | | | | | ↑ | L | Rank B | ↑ | H | QoB |
| | | | | | | ↑ | H | QoA | UC | X | QoB |
| | | | | | | ↑ | H | QoA | ↑ | L | B bus |
| | | | | | | ↑ | H | QoA | ↑ | H | QoB |
| A-to-B Operation | L | H | Input | Output of Rank A | | UC | X | QoA | UC | X | QoB |
| | | | | | | UC | X | QoA | ↑ | L | Rank A |
| | | | | | | UC | X | QoA | ↑ | H | QoB |
| | | | | | | ↑ | L | A bus | UC | X | QoB |
| | | | | | | ↑ | L | A bus | ↑ | L | Rank A |
| | | | | | | ↑ | L | A bus | ↑ | H | QoB |
| | | | | | | ↑ | H | QoA | UC | X | QoB |
| | | | | | | ↑ | H | QoA | ↑ | L | Rank A |
| | | | | | | ↑ | H | QoA | ↑ | H | QoB |
| Transfer Stored Data | L | L | Output of Rank B | Output of Rank A | | UC | X | QoA | UC | X | QoB |
| | | | | | | UC | X | QoA | ↑ | L | Rank A |
| | | | | | | UC | X | QoA | ↑ | H | QoB |
| | | | | | | ↑ | L | Rank B | UC | X | QoB |
| | | | | | | ↑ | L | Rank B | ↑ | L | Rank A |
| | | | | | | ↑ | L | Rank B | ↑ | H | QoB |
| | | | | | | ↑ | H | QoA | UC | X | QoB |
| | | | | | | ↑ | H | QoA | ↑ | L | Rank A |
| | | | | | | ↑ | H | QoA | ↑ | H | QoB |

Bus Operation For 'LS567

| OPERATION | DIRECTION CONTROL | | DATA I/O | | BLOCK DIAGRAM | GATE ENABLE (A) | | RANK A | GATE ENABLE (B) | | RANK B |
|----------------------|-------------------|------|------------------|------------------|---------------|-----------------|-----|--------|-----------------|-----|--------|
| | OEAB | OEBA | A0-A7 | B0-B7 | | GA1 | GA2 | | GB1 | GB2 | |
| | Storage | H | H | Input | | Input | | L | H | QoA | L |
| L | | | | | H | | | QoA | H | X | B bus |
| L | | | | | H | | | QoA | X | L | B bus |
| H | | | | | X | | | A bus | L | H | QoB |
| H | | | | | X | | | A bus | H | X | B bus |
| H | | | | | X | | | A bus | X | L | B bus |
| X | | | | | L | | | A bus | L | H | QoB |
| X | | | | | L | | | A bus | H | X | B bus |
| X | | | | | L | | | A bus | X | L | B bus |
| B-to-A Operation | H | L | Output of Rank B | Input | | L | H | QoA | L | H | QoB |
| | | | | | | L | H | QoA | H | X | B bus |
| | | | | | | L | H | QoA | X | L | B bus |
| | | | | | | H | X | Rank B | L | H | QoB |
| | | | | | | H | X | Rank B | H | X | B bus |
| | | | | | | H | X | Rank B | X | L | B bus |
| | | | | | | X | L | Rank B | L | H | QoB |
| | | | | | | X | L | Rank B | H | X | B bus |
| | | | | | | X | L | Rank B | X | L | B bus |
| A-to-B Operation | L | H | Input | Output of Rank A | | L | H | QoA | L | H | QoB |
| | | | | | | L | H | QoA | H | X | Rank A |
| | | | | | | L | H | QoA | X | L | Rank A |
| | | | | | | H | X | A bus | L | H | QoB |
| | | | | | | H | X | A bus | H | X | Rank A |
| | | | | | | H | X | A bus | X | L | Rank A |
| | | | | | | X | L | A bus | L | H | QoB |
| | | | | | | X | L | A bus | H | X | Rank A |
| | | | | | | X | L | A bus | X | L | Rank A |
| Transfer Stored Data | L | L | Output of Rank B | Output of Rank A | | L | H | QoA | L | H | QoB |
| | | | | | | L | H | QoA | H | X | Rank A |
| | | | | | | L | H | QoA | X | L | Rank A |
| | | | | | | H | X | Rank B | L | H | QoB |
| | | | | | | H* | X | Rank B | H | X | Rank A |
| | | | | | | H* | X | Rank B | X | L | Rank A |
| | | | | | | X | L | Rank B | L | H | QoB |
| | | | | | | X* | L | Rank B | H | X | Rank A |
| | | | | | | X* | L | Rank B | X | L | Rank A |

* NOTE: These controls for OEAB, OEBA, GA1, GA2, GB1 and GB2 can cause race conditions.

Absolute Maximum Ratings

| | |
|--------------------------------|-----------------|
| Supply voltage V_{CC} | -0.5 V to 7 V |
| Input voltage | -1.5 V to 7 V |
| Off-state output voltage | -0.5 V to 5.5 V |
| Storage temperature | -65°C to +150°C |

Operating Conditions

| SYMBOL | PARAMETER | | | | MILITARY | | | COMMERCIAL | | | UNIT |
|------------|---|----------------|----------------------------------|----------------------------------|----------|-----|-----|------------|-----|------|------|
| | | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{CC} | Supply voltage | | | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| T_A | Operating free-air temperature | | | | -55 | | 125 | 0 | | 75 | °C |
| T_W | Width of clock/gate | 'LS546, 'LS566 | High | CK | 11 | | | 8 | | | ns |
| | | | Low | | 19 | | | 15 | | | |
| | | 'LS547, 'LS567 | High | GA1, GB1 | 10 | | | 8 | | | |
| | | | Low | $\overline{GA2}, \overline{GB2}$ | 18 | | | 16 | | | |
| T_{su} | Setup time | 'LS546 | CKA, CKB | | 14↓ | | | 11↓ | | | ns |
| | | 'LS547 | GA1, GB1 | | 5↓ | | | 5↓ | | | |
| | | | $\overline{GA2}, \overline{GB2}$ | | 15↓ | | | 15↓ | | | |
| | | 'LS566 | CKA, CKB | | 14↓ | | | 11↓ | | | |
| | | 'LS567 | GA1, GB1 | | 13↓ | | | 13↓ | | | |
| | | | $\overline{GA2}, \overline{GB2}$ | | 22↓ | | | 22↓ | | | |
| T_h | Hold time | 'LS546 | CKA, CKB | | 0↑ | | | 0↑ | | | ns |
| | | 'LS547 | GA1, GB1 | | 13↓ | | | 13↓ | | | |
| | | | $\overline{GA2}, \overline{GB2}$ | | 5↑ | | | 5↑ | | | |
| | | 'LS566 | CKA, CKB | | 0↑ | | | 0↑ | | | |
| | | 'LS567 | GA1, GB1 | | 11↓ | | | 11↓ | | | |
| | | | $\overline{GA2}, \overline{GB2}$ | | 5↑ | | | 5↑ | | | |
| T_{suce} | Setup time for $\overline{CKEA}, \overline{CKEB}$, ('LS546, 'LS566 only) | | | | 15↓ | | | 11↓ | | | ns |
| T_{hce} | Hold time for $\overline{CKEA}, \overline{CKEB}$ ('LS546, 'LS566 only) | | | | 5↑ | | | 4↑ | | | ns |

- ↓ the arrow indicates the transition of the clock/gate input used for reference:
 ↑ for the low-to-high transitions.
 ↓ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY | | | COMMERCIAL | | | UNIT |
|------------------|-------------------------------|--|---------------------------|-----|------|------------------------|------|------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IL} | Low-level input voltage | | | | 0.8 | | 0.8 | | V |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | | V |
| V _{IC} | Input clamp voltage | V _{CC} = MIN I _I = -18 mA | | | -1.5 | | -1.5 | | V |
| I _{IL} | Low-level input current | V _{CC} = MAX V _I = 0.4 V | A or B | | -250 | | -250 | | μA |
| | | | All others | | -400 | | -400 | | |
| I _{IH} | High-level input current | V _{CC} = MAX V _I = 2.7 V | | | 20 | | 20 | | μA |
| I _I | Maximum input current | V _{CC} = MAX | A or B | | 0.1 | | 0.1 | | mA |
| | | | All others | | | V _I = 7.0 V | | | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN V _{IL} = MAX V _{IH} = 2V | I _{OL} = 24 mA | | 0.5 | | | | V |
| | | | I _{OL} = 32 mA | | | 0.35 | 0.5 | | |
| V _{OH} | High-level output voltage | V _{CC} = MIN V _{IL} = MAX V _{IH} = 2V | I _{OH} = -1 mA | 2.4 | 3.4 | | | | V |
| | | | I _{OH} = -2.6 mA | | | 2.4 | 3.1 | | |
| I _{OZL} | Off-state output current | V _{CC} = MAX | V _O = 0.4 V | | -250 | | -250 | | μA |
| I _{OZH} | | | V _O = 2.4 V | | 20 | | 20 | | |
| I _{OS} | Output short-circuit current* | V _{CC} = MAX | | -30 | -130 | | -30 | -130 | mA |
| I _{CC} | Supply current | V _{CC} = MAX Outputs open | 'LS546 | | 180 | | 180 | | mA |
| | | | 'LS547 | | 180 | | 180 | | |
| | | | 'LS566 | | 180 | | 180 | | |
| | | | 'LS567 | | 180 | | 180 | | |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

SN54/74LS546 SN54/74LS547

Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY | | COMMERCIAL | | UNIT | | |
|------------------------------------|---|--|---------------|---------------|---------------|---------------|------|---------------|---------------|
| | | | 'LS546 MIN | 'LS546 MAX | 'LS547 MIN | 'LS547 MAX | | 'LS546 MIN | 'LS546 MAX |
| f _{MAX} | Maximum clock frequency | C _L = 45 pF R _L = 280 Ω $\overline{OE} = L$ | 33 | | | 43 | | MHz | |
| t _{PLH} /t _{PHL} | CK to output delay ('LS546 only) | | 26 | | | 21 | | ns | |
| t _{PLH} /t _{PHL} | GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only) | | | | 27 | | | 24 | ns |
| t _{PLH} /t _{PHL} | Data D to output delay ('LS547 only) | | | | 23 | | | 18 | ns |
| t _{PZL} /t _{PZH} | Output enable delay | C _L = 45 pF R _L = 280 Ω | 25 | 25 | | 21 | 21 | ns | |
| t _{PLZ} /t _{PHZ} | Output disable delay | C _L = 5 pF R _L = 280 Ω | 22 | 22 | | 19 | 19 | ns | |

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

| SYMBOL | PARAMETER | TEST CONDITIONS | 'LS546 | | 'LS547 | | UNIT |
|------------------------------------|---|--|--------|-----|--------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| f _{MAX} | Maximum clock frequency | C _L = 45 pF R _L = 280 Ω $\overline{OE} = L$ | | 50 | | | MHz |
| t _{PLH} /t _{PHL} | CK to output delay ('LS546 only) | | | 19 | | | ns |
| t _{PLH} /t _{PHL} | GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only) | | | | | 23 | ns |
| t _{PLH} /t _{PHL} | Data D to output delay ('LS547 only) | | | | | 17 | ns |
| t _{PZL} /t _{PZH} | Output enable delay | C _L = 45 pF R _L = 280 Ω | | 19 | | 19 | ns |
| t _{PLZ} /t _{PHZ} | Output disable delay | C _L = 5 pF R _L = 280 Ω | | 17 | | 17 | ns |

13

Switching Characteristics Over Operating Conditions

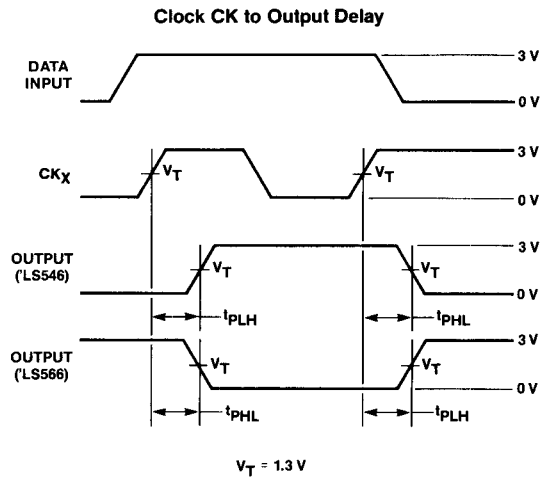
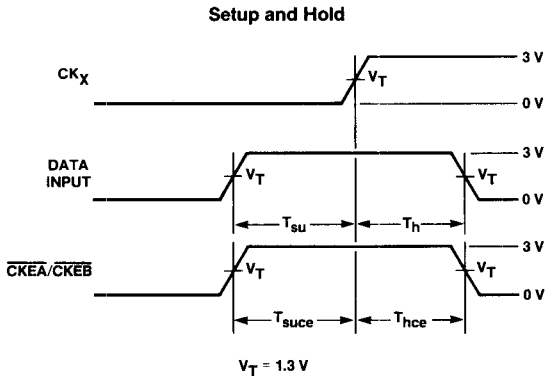
| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY | | COMMERCIAL | | UNIT |
|------------------------------------|--|--|---------------|---------------|---------------|---------------|------|
| | | | 'LS566 MIN | 'LS566 MAX | 'LS567 MIN | 'LS567 MAX | |
| f _{MAX} | Maximum clock frequency | C _L = 45 pF R _L = 280 Ω $\overline{OE} = L$ | 33 | | 43 | | MHz |
| t _{PLH} /t _{PHL} | CK to output delay ('LS566 only) | | 26 | | 21 | | ns |
| t _{PLH} /t _{PHL} | GA1, GA2, GB1 or GB2 to output delay ('LS567 only) | | | 26 | | 24 | ns |
| t _{PLH} /t _{PHL} | Data D to output delay ('LS567 only) | | | 29 | | 23 | ns |
| t _{PZL} /t _{PZH} | Output enable delay | C _L = 45 pF R _L = 280 Ω | 25 | 25 | 21 | 21 | ns |
| t _{PLZ} /t _{PHZ} | Output disable delay | C _L = 5 pF R _L = 280 Ω | 22 | 22 | 19 | 19 | ns |

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

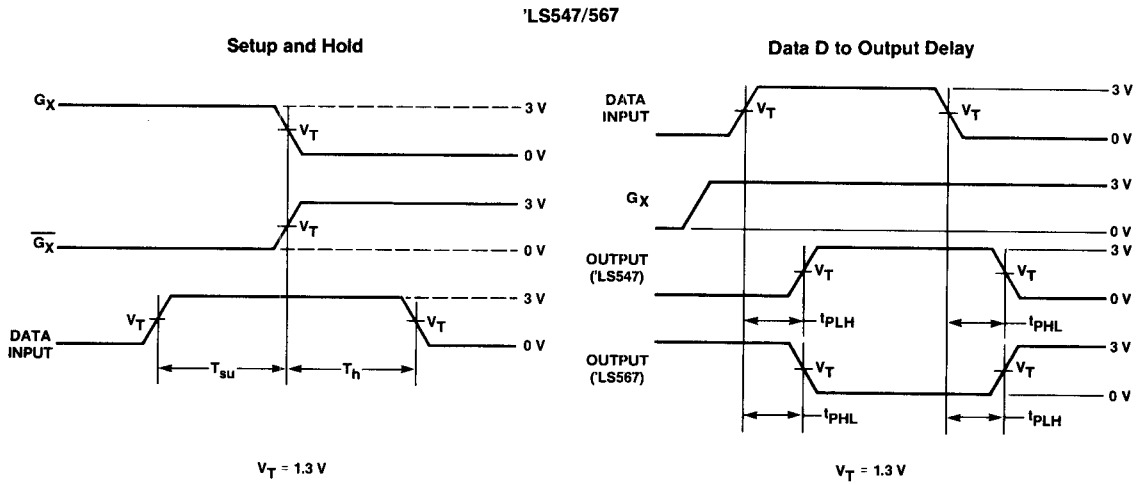
| SYMBOL | PARAMETER | TEST CONDITIONS | 'LS566 | | 'LS567 | | UNIT |
|------------------------------------|--|--|--------|-----|--------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| f _{MAX} | Maximum clock frequency | C _L = 45 pF R _L = 280 Ω $\overline{OE} = L$ | | 50 | | | MHz |
| t _{PLH} /t _{PHL} | CK to output delay ('LS566 only) | | | 19 | | | ns |
| t _{PLH} /t _{PHL} | GA1, GA2, GB1 or GB2 to output delay ('LS567 only) | | | | | 21 | ns |
| t _{PLH} /t _{PHL} | Data D to output delay ('LS567 only) | | | | | 19 | ns |
| t _{PZL} /t _{PZH} | Output enable delay | C _L = 45 pF R _L = 280 Ω | | 19 | | 19 | ns |
| t _{PLZ} /t _{PHZ} | Output disable delay | C _L = 5 pF R _L = 280 Ω | | 17 | | 17 | ns |

Definition of Waveforms

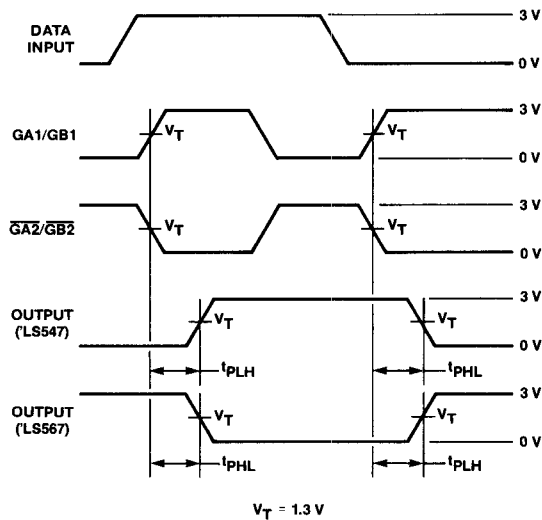
'LS546/566



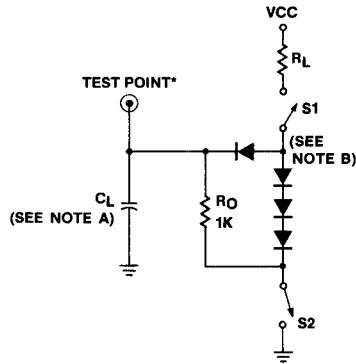
Definition of Waveforms



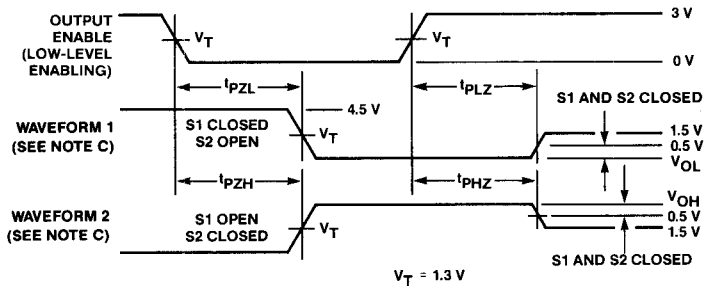
GA1, GA2, GB1 or GB2 to Output Delay



Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



ENABLE AND DISABLE

- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N916 or 1N3064.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
 E. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{Out} = 50\Omega$ and $t_R \leq 15$ ns $t_F \leq 6$ ns.
 F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.