

October 1987 Revised April 2002

CD4512BC 8-Channel Buffered Data Selector

General Description

The CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a 3-STATE output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable (OE) input forces the output into the 3-STATE condition. Low levels at both the Inhibit and (\overline{OE}) inputs allow normal operation.

Features

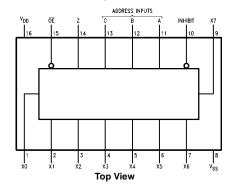
- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- 3-STATE output
- Low quiescent power dissipation: 0.25 μ W/package (typ.) @ V_{CC} = 5.0V
- Plug-in replacement for Motorola MC14512

Ordering Code:

Order Number	Package Number	Package Description
CD4512BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4512BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending suffix "X" to the ordering code.

Connection Diagram



Truth Table

Address Inputs			Control I	Output	
C	В	Α	Inhibit	OE.	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0 0 X2	
0	1	1	0	0	Х3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
2	1	1	1	0	0
2	2	2	2	1	Hi-Z

2 = Don't care

Hi-Z = 3-STATE condition

Xn = Data at input n

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Absolute Maximum Ratings(Note 1)

(Note 2)

 $\begin{array}{cc} \text{Supply Voltage (V}_{\text{DD}}) & -0.5 \text{ to } +18 \text{ V}_{\text{DO}} \\ \text{Input Voltage (V}_{\text{IN}}) & -0.5 \text{ to } \text{V}_{\text{DD}} + 0.5 \text{ V}_{\text{DO}} \end{array}$

Storage Temperature Range (T_S) $-65^{\circ}C$ to $+150^{\circ}C$

Power Dissipation (P_D)

Dual-In-Line 700 mW Small Outline 500 mW

Lead Temperature, (T_L)

(Soldering, 10 seconds) 260°C

Recommended Operating Conditions (Note 2)

 $\begin{array}{ccc} -0.5 \text{ to } +18 \text{ V}_{DC} & \text{DC Supply Voltage (V}_{DD}) & 3.0 \text{ to } 15 \text{ V}_{DC} \\ -0.5 \text{ to V}_{DD} + 0.5 \text{ V}_{DC} & \text{Input Voltage (V}_{IN}) & 0 \text{ to V}_{DD} \text{ V}_{DC} \\ -65^{\circ}\text{C to } +150^{\circ}\text{C} & \text{Operating Temperature Range (T}_{A}) & -55^{\circ}\text{C to } +125^{\circ}\text{C} \end{array}$

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The Recommended Operating Conditions and Electrical Characteristics table provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

Parameter	Conditions	–55°C		+25°C			+125°C		Units
	Conditions		Max	Min	Тур	Max	Min	Max	Units
Quiescent Device	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5		0.005	5		150	
Current	$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.010	10		300	μΑ
	$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.015	20		600	
LOW Level	$V_{DD} = 5V$		0.05		0	0.05		0.05	
Output Voltage	$V_{DD} = 10V$ $ I_{OL} < 1 \mu A$		0.05		0	0.05		0.05	V
	$V_{DD} = 15V$		0.05		0	0.05		0.05	
HIGH Level	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		
Output Voltage	$V_{DD} = 10V$ $ I_{OH} < 1 \mu A$	9.95		9.95	10.0		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15.0		14.95		
LOW Level	$V_{DD} = 5V, V_{O} = 0.5V$		1.5		2.25	1.5		1.5	
Input Voltage	$V_{DD} = 10V, V_{O} = 1.0V$		3.0		4.50	3.0		3.0	V
	$V_{DD} = 15V, V_{O} = 1.5V$		4.0		6.75	4.0		4.0	
HIGH Level	$V_{DD} = 5V, V_{O} = 4.5V$	3.5		3.5	2.75		3.5		
Input Voltage	$V_{DD} = 10V, V_{O} = 9.0V$	7.0		7.0	5.50		7.0		V
	$V_{DD} = 15V, V_{O} = 13.5V$	11.0		11.0	8.25		11.0		
LOW Level Output	$V_{DD} = 5V, V_{O} = 0.4V$	0.64		0.51	0.78		0.36		
Current	$V_{DD} = 10V, V_{O} = 0.5V$	1.6		1.3	2.0		0.9		mA
(Note 3)	$V_{DD} = 15V, V_{O} = 1.5V$	4.2		3.4	7.8		2.4		
HIGH Level Output	$V_{DD} = 5V, V_{O} = 4.6V$	-0.25		-0.2			-0.14		
Current	$V_{DD} = 10V, V_{O} = 9.5$	-0.62		-0.5			-0.35		mA
(Note 3)	$V_{DD} = 15V$, $V_{O} = 13.5V$	-1.8		-1.5			-1.1		
Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10 ⁻⁵	-0.1		-1.0	μА
	$V_{DD} = 15V, V_{IN} = 15V$		0.1		10 ⁻⁵	0.1		1.0	μΑ
3-STATE	$V_{DD} = 15V, V_{O} = 0V$		±1.0		±10 ⁻⁵	±1.0		±3.0	μΑ
Output Current	$V_{DD} = 15V, V_{O} = 15V$								
	Quiescent Device Current LOW Level Output Voltage HIGH Level Output Voltage LOW Level Input Voltage HIGH Level Input Voltage LOW Level Output Current (Note 3) HIGH Level Output Current (Note 3) Input Current 3-STATE	Quiescent Device $V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS} Current $V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS} LOW Level $V_{DD} = 5V$ Output Voltage $V_{DD} = 10V$ $ I_{OL} < 1 \mu A$ HIGH Level $V_{DD} = 5V$ Output Voltage $V_{DD} = 10V$ $ I_{OH} < 1 \mu A$ V _{DD} = 15V $V_{DD} = 15V$ LOW Level $V_{DD} = 5V$, $V_{O} = 0.5V$ Input Voltage $V_{DD} = 10V$, $V_{O} = 1.0V$ V _{DD} = 15V, $V_{O} = 1.5V$ $V_{DD} = 15V$, $V_{O} = 4.5V$ Input Voltage $V_{DD} = 15V$, $V_{O} = 9.0V$ V _{DD} = 15V, $V_{O} = 1.5V$ $V_{DD} = 15V$, $V_{O} = 0.5V$ LOW Level Output $V_{DD} = 5V$, $V_{O} = 0.5V$ (Note 3) $V_{DD} = 15V$, $V_{O} = 1.5V$ HIGH Level Output $V_{DD} = 5V$, $V_{O} = 4.6V$ Current $V_{DD} = 15V$, $V_{O} = 9.5$ (Note 3) $V_{DD} = 15V$, $V_{O} = 13.5V$ Input Current $V_{DD} = 15V$, $V_{O} = 13.5V$ Input Current $V_{DD} = 15V$, $V_{O} = 0.5V$ $V_{DD} = 15V$, $V_{O} = 15V$ $V_{DD} = 15V$, $V_{O} $	Parameter Conditions Min	Parameter Conditions Min Max	Parameter Conditions Min Max Min	Parameter Conditions Min Max Min Typ	Parameter Conditions Min Max Min Typ Max	Conditions Min Max Min Typ Max Min Mi	Parameter Conditions Min Max Min Typ Max Min Max Max Max Max Max Max Max Max Ma

Note 3: $\rm I_{OH}$ and $\rm I_{OL}$ are tested one output at a time.

AC Electrical Characteristics (Note 4) $T_A = 25^{\circ}C, \ t_r = t_f = 20 \ ns, \ C_L = 50 \ pF$

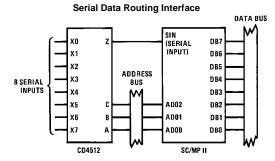
Symbol	Parameter	Conditions		CD4512BM			CD4512BC		
Symbol			Min	Тур	Max	Min	Тур	Max	Units
t _{PHL}	Propagation Delay	$V_{DD} = 5V$		225	500		225	750	
	HIGH-to-LOW Level	$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	
t _{PLH}	Propagation Delay	$V_{DD} = 5V$		225	500		225	750	
	LOW-to-HIGH Level	$V_{DD} = 10V$		75	175		75	200	ns
		$V_{DD} = 15V$		57	130		57	150	
t _{THL} , t _{TLH}	Transition Time	$V_{DD} = 5V$		70	200		70	200	
		$V_{DD} = 10V$		35	100		35	100	ns
		$V_{DD} = 15V$		25	80		25	80	
t _{PHZ} , t _{PLZ}	Propagation Delay into	$V_{DD} = 5V$		50	125		50	125	
	3-STATE from Logic Level	$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	
t_{PZH} , t_{PZL}	Propagation Delay to Logic	$V_{DD} = 5V$		50	125		50	125	
	Level from 3-STATE	$V_{DD} = 10V$		25	75		25	75	ns
		$V_{DD} = 15V$		19	60		19	60	
C _{IN}	Input Capacitance	(Note 5)		7.5	15		7.5	15	pF
C _{OUT}	3-STATE Output Capacitance	(Note 5)		7.5	15		7.5	15	pF
C _{PD}	Power Dissipation Capacity	(Note 6)		150			150		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

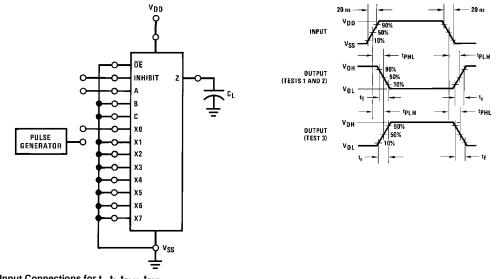
Note 5: Capacitance guaranteed by periodic testing.

Note 6: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see Family Characteristics Application Note, AN-90.

Typical Application



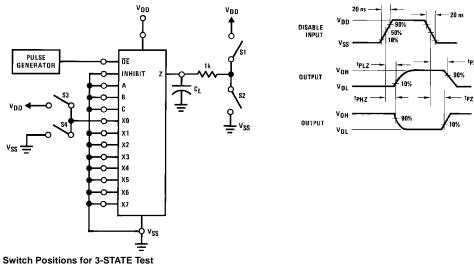
AC Test Circuit and Switching Time Waveforms



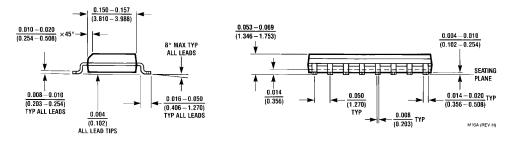
Input Connections for $\mathbf{t_r},\,\mathbf{t_f},\,\mathbf{t_{PLH}},\,\mathbf{t_{PHL}}$

Test	Inhibit	Α	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

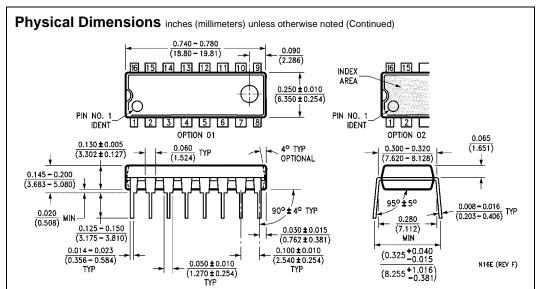
3-STATE AC Test Circuit and Switching Time Waveforms



Test	S1	S2	S3	S4
t _{PHZ}	Open	Closed	Closed	Open
t _{PLZ}	Closed	Open	Open	Closed
t _{PZL}	Closed	Open	Open	Closed
t _{PZH}	Open	Closed	Closed	Open



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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