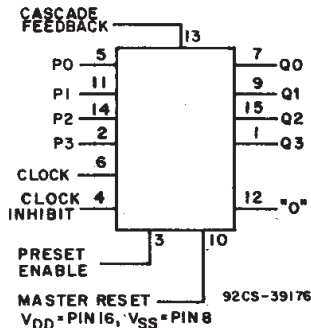


NOT RECOMMENDED FOR NEW DESIGNS

# CD4522B Types

Advance Information/  
Preliminary Data



**FUNCTIONAL DIAGRAM**

## CMOS Programmable BCD Divide-by-“N” Counter High-Voltage Types (20-Volt Rating)

**Features:**

- Internally synchronous for high internal and external speeds.
- Logic edge-clocked design — increments on positive Clock transition or on negative Clock Inhibit transition.
- 100% tested for quiescent current at 20-V.
- 5-V, 10-V, and 15-V parametric ratings.

- Standard symmetrical output characteristics.
- Maximum input current of 1  $\mu$ A at 18 V over full package-temperature range: 100 nA at 18 V and 25° C.
- Meets all requirements of JEDEC Standard No. 13B, “Standard Specifications for Description of ‘B’ Series CMOS Devices.”

■ CD4522B programmable BCD counter has a decoded “0” state output for divide-by-N applications. In single stage operation the “0” output is tied to the Preset Enable input. The Cascade Feedback allows multiple stage divide-by-N operation without the need for external gating. A HIGH on the Clock Inhibit disables the pulse-counting function. A HIGH on the Master Reset asynchronously resets the divide-by-N operation. The output is presented in BCD format.

**Applications:**

- Frequency synthesizers
- Phase-locked loops
- Programmable down counters
- Programmable frequency dividers

The CD4522B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

**MAXIMUM RATINGS, Absolute-Maximum Values:**

**DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)**

Voltages referenced to V<sub>SS</sub> Terminal) ..... -0.5V to +20V

**INPUT VOLTAGE RANGE, ALL INPUTS** ..... -0.5V to V<sub>DD</sub> +0.5V

**DC INPUT CURRENT, ANY ONE INPUT** .....  $\pm$ 10mA

**POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):**

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

**DEVICE DISSIPATION PER OUTPUT TRANSISTOR**

FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

**OPERATING-TEMPERATURE RANGE (T<sub>A</sub>)** ..... -55°C to +125°C

**STORAGE TEMPERATURE RANGE (T<sub>stg</sub>)** ..... -65°C to +150°C

**LEAD TEMPERATURE (DURING SOLDERING):**

At distance 1/16  $\pm$  1/32 inch (1.59  $\pm$  0.79mm) from case for 10s max ..... +265°C

3  
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HIGH VOLTAGE ICs

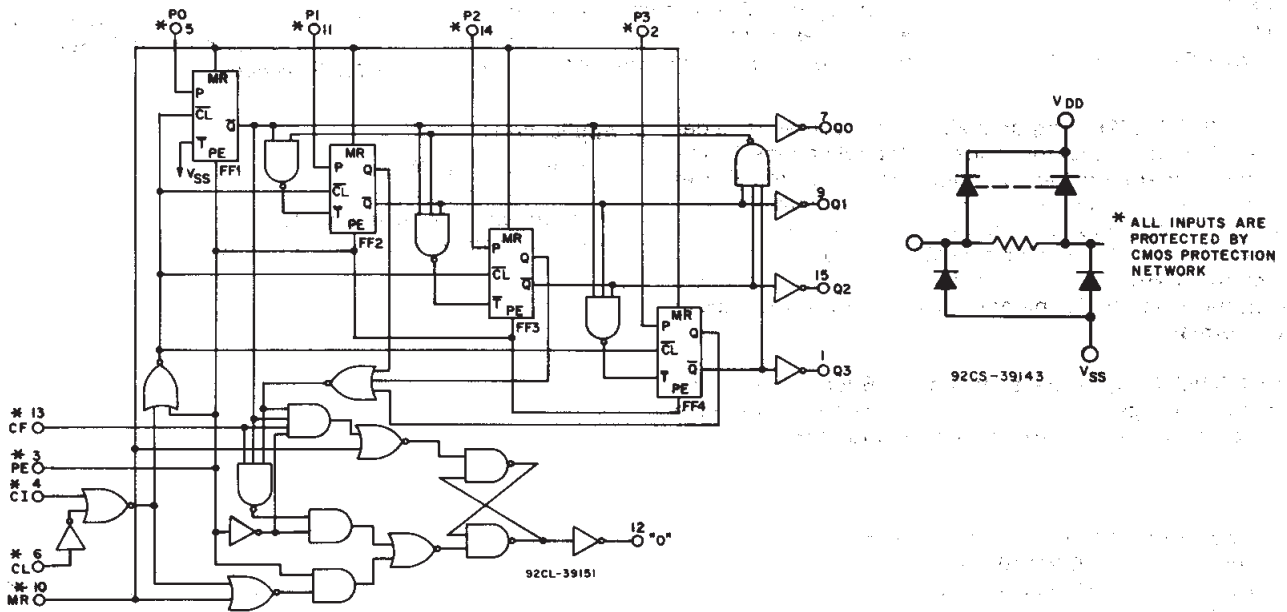
# CD4522B Types

## TRUTH TABLES

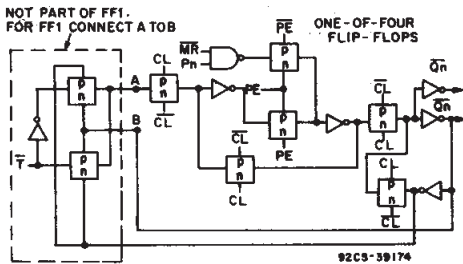
CLOCK	CLOCK INHIBIT	PRESET ENABLE	MASTER RESET	ACTION
0	0	0	0	No Count
0	0	0	0	Count Down
X	1	0	0	No Count
1	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

Count	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1



a. Basic diagram.



b. Flip-flop detail.

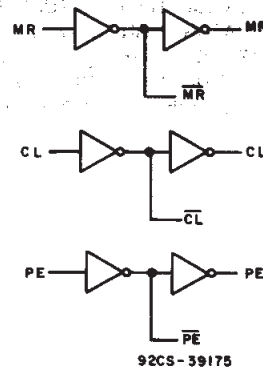


Fig. 1 - Logic diagram for the CD4522B.

## CD4522B Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ , except as noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	$V_{DD}$ (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)		3	18	V
Pulse Width:	5	250	—	ns
	10	100	—	
	15	80	—	
Clock, $t_{w(cc)}$	5	250	—	ns
	10	100	—	
	15	80	—	
Preset Enable, $t_{w(cc)}$	5	250	—	ns
	10	100	—	
	15	80	—	
Master Reset, $t_{w(MR)}$	5	350	—	ns
	10	250	—	
	15	200	—	
Clock Frequency, $f_{CL}$	5	—	1.5	MHz
	10	—	3.0	
	15	—	4.0	
Clock Rise and Fall Time $t_{rCL}, t_{fCL}$	5	—	15	$\mu\text{s}$
	10	—	15	
	15	—	15	
Preset Enable Set-up Time, $t_{su}$	5	0	—	ns
	10	0	—	
	15	0	—	
Preset Enable Hold Time, $t_h$	5	75	—	ns
	10	25	—	
	15	20	—	
Master Reset Removal Time, $t_{rem}$	5	130	—	ns
	10	50	—	
	15	30	—	

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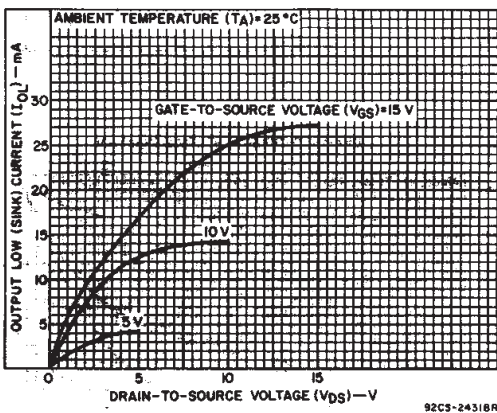


Fig. 2 — Typical output low (sink) current characteristics.

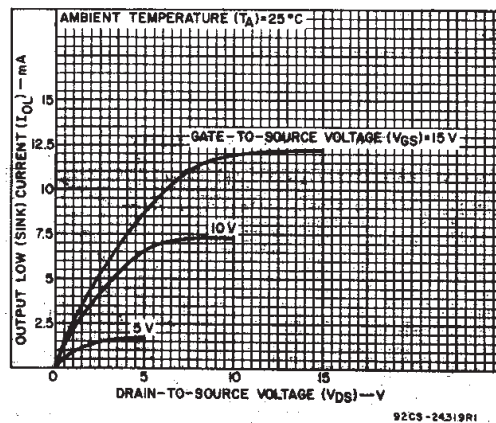


Fig. 3 — Minimum output low (sink) current characteristics.

# CD4522B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	+25							
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0, 10	10	10	10	300	300	—	0.04	10	
	—	0, 15	15	20	20	600	600	—	0.04	20	
	—	0, 20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
Output High (Source) Current, I <sub>OH</sub> Min.	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	mA
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
	—	0, 5	5	0.05				—	0	0.05	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0, 10	10	0.05				—	0	0.05	V
	—	0, 15	15	0.05				—	0	0.05	
	—	0, 5	5	4.95				4.95	5	—	
Output Voltage: High-Level V <sub>OH</sub> Min.	—	0, 10	10	9.95				9.95	10	—	V
	—	0, 15	15	14.95				14.95	15	—	
	0.5, 4.5	—	5	1.5				—	—	1.5	
Input low Voltage, V <sub>IL</sub> Max.	1, 9	—	10	3				—	—	3	V
	1.5, 13.5	—	15	4				—	—	4	
	0.5, 4.5	—	5	3.5				3.5	—	—	
Input High Voltage, V <sub>IH</sub> Min.	1, 9	—	10	7				7	—	—	V
	1.5, 13.5	—	15	11				11	—	—	
	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	

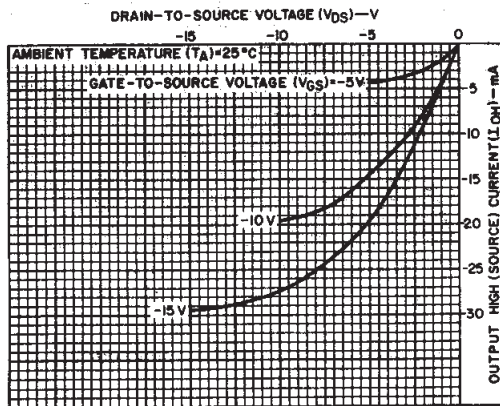


Fig. 4 — Typical output high (source) current characteristics.

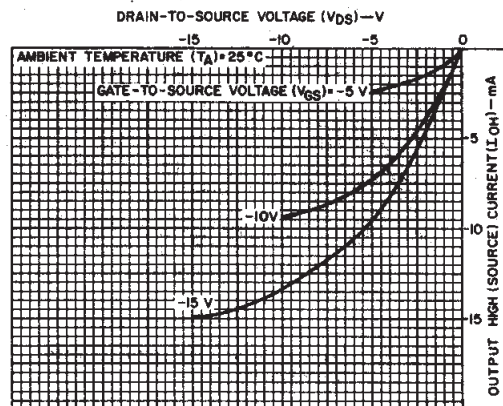


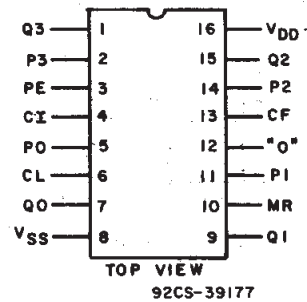
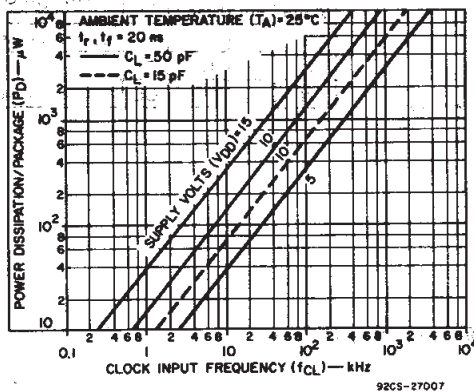
Fig. 5 — Minimum output high (source) current characteristics.

## CD4522B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ , Input  $t_r, t_f = 20\text{ ns}$ ,  $C_i = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$**

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		$V_{DD}$ (V)	Min.	Typ.		Max.
Propagation Delay Time; $t_{PHL}, t_{PLH}$ Clock to "Q" outputs		5	—	550	1100	ns
		10	—	225	450	
		15	—	160	320	
Clock to "0" output		5	—	420	710	ns
		10	—	160	270	
		15	—	110	190	
Clock inhibit to "Q" outputs		5	—	270	540	ns
		10	—	100	200	
		15	—	70	140	
Master reset to "Q" outputs		5	—	270	540	ns
		10	—	100	200	
		15	—	70	140	
Preset Enable Setup Time, $t_{su}$		5	—	0	0	ns
		10	—	0	0	
		15	—	0	0	
Preset Enable Hold Time, $t_h$		5	—	75	150	ns
		10	—	25	50	
		15	—	20	40	
Master Reset Removal Time, $t_{rem}$		5	—	130	260	ns
		10	—	50	100	
		15	—	30	60	
Transition Time, $t_{THL}, t_{TLH}$		5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Minimum Pulse Width Clock, $t_{W(CL)}$		5	—	125	250	ns
		10	—	50	100	
		15	—	40	80	
Preset Enable, $t_{W(PE)}$		5	—	125	250	ns
		10	—	50	100	
		15	—	40	80	
Master Reset, $t_{W(MR)}$		5	—	175	350	ns
		10	—	125	250	
		15	—	100	200	
Max Clock Freq, $f_{CL}$		5	—	3	1.5	MHz
		10	—	6	3.0	
		15	—	8	4.0	
Max Clock or Clock Inhibit Rise & Fall Time, $t_{TLH}, t_{THL}$		5	—	—	15	us
		10	—	—	15	
		15	—	—	15	
Input Capacitance, $C_{IN}$	Any Input	—	—	5	7.5	pF

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**TERMINAL ASSIGNMENT**

**Fig. 6 — Typical dynamic power dissipation vs. frequency.**

## CD4522B Types

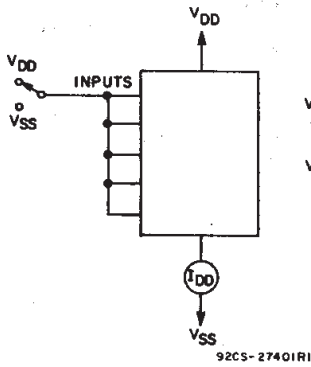


Fig. 7 — Quiescent device current test circuit.

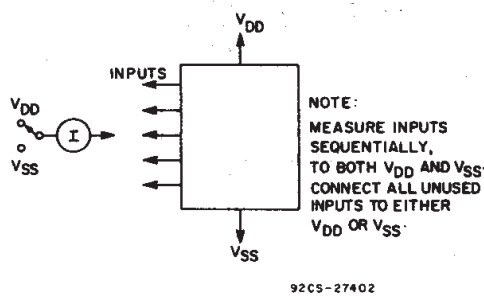


Fig. 8 — Input current test circuit.

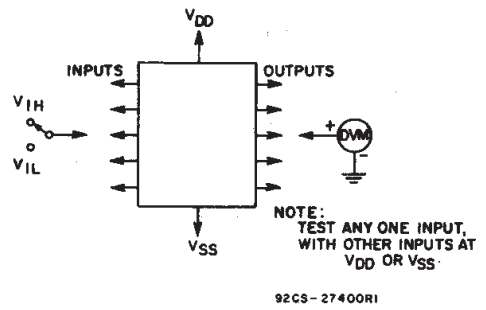


Fig. 9 — Input voltage test circuit.

## APPLICATION CIRCUITS

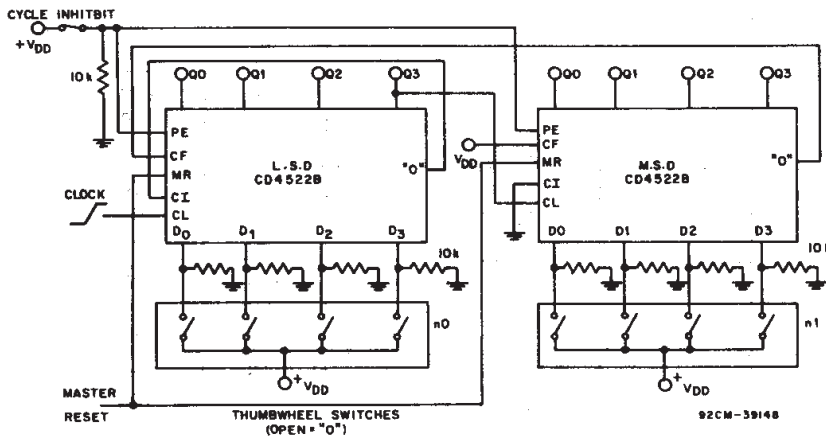


Fig. 10 — 2-Stage Programmable Down Counter (One Cycle)

From		To		Range of N
Stage	Pin	Stage	Pin	
LSD	"0"	All	PE	LSD < N < MSD
N	"0"	N-1	CF	LSD + 1 < N < MSD
N	"0 <sub>3</sub> "	N+1	CL	LSD < N < MSD-1

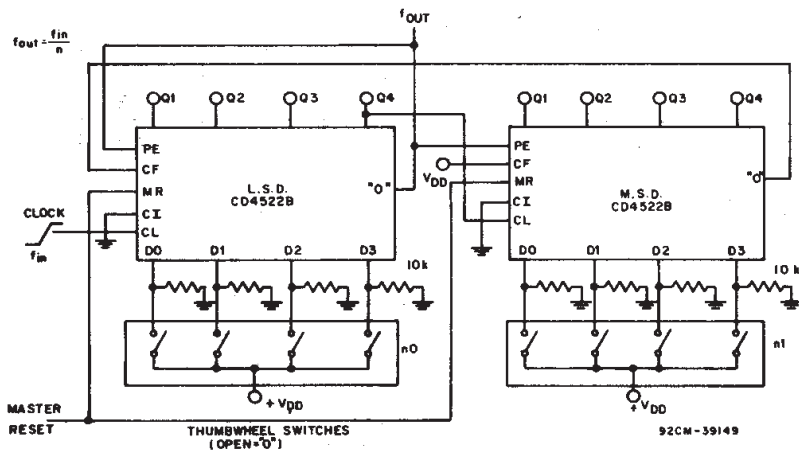
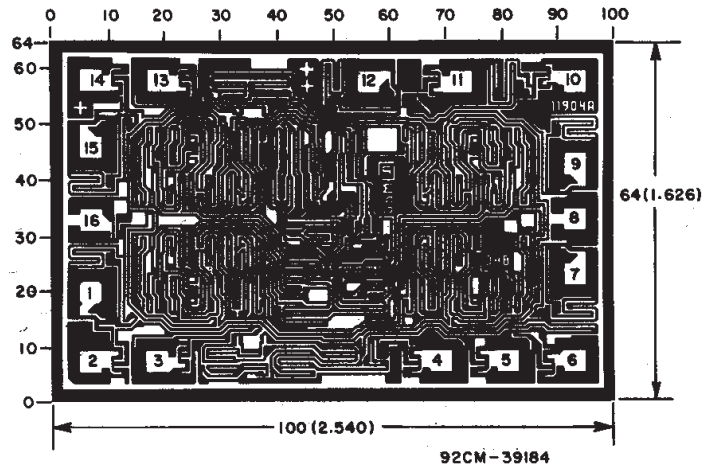


Fig. 11 — 2-Stage Programmable Frequency Divider

From		To		Range of N
Stage	Pin	Stage	Pin	
LSD	"0"	All	PE	LSD < N < MSD
N	"0"	N-1	CF	LSD + 1 < N < MSD
N	"0 <sub>3</sub> "	N+1	CL	LSD < N < MSD-1

## CD4522B Types



*Dimensions and pad layout for CD4522BH.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

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