

TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44,  
SN54LS42, SN7442A THRU SN7444A, SN74LS42  
4-LINE TO 10-LINE DECODERS (1-OF-10)

MARCH 1974 - REVISED APRIL 1985

'42A, 'L42, 'LS42 ... BCD-TO-DECIMAL  
'43A, 'L43 ... EXCESS-3-TO-DECIMAL  
'44A, 'L44 ... GRAY-TO-DECIMAL

- All Outputs Are High for Invalid Input Conditions
- Also for Application as  
4-Line-to-16-Line Decoders  
3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'L42, 'L43, 'L44	70 mW	49 ns
'LS42	35 mW	17 ns

**description**

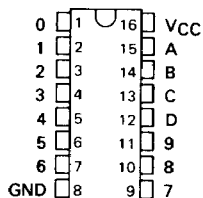
These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

Series 54, 54L, and 54LS circuits are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74, and 74LS circuits are characterized for operation from 0°C to 70°C.

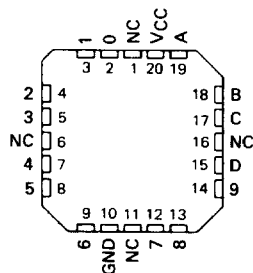
SN5442A THRU SN5444A, SN54LS42 ... J OR W PACKAGE  
SN54L42 THRU SN54L44 ... J PACKAGE  
SN7442A THRU SN7444A ... J OR N PACKAGE  
SN74LS42 ... D, J OR N PACKAGE

(TOP VIEW)



SN54LS42 ... FK PACKAGE  
SN74LS42 ... FN PACKAGE

(TOP VIEW)



NC - No internal connection

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**PRODUCTION DATA**

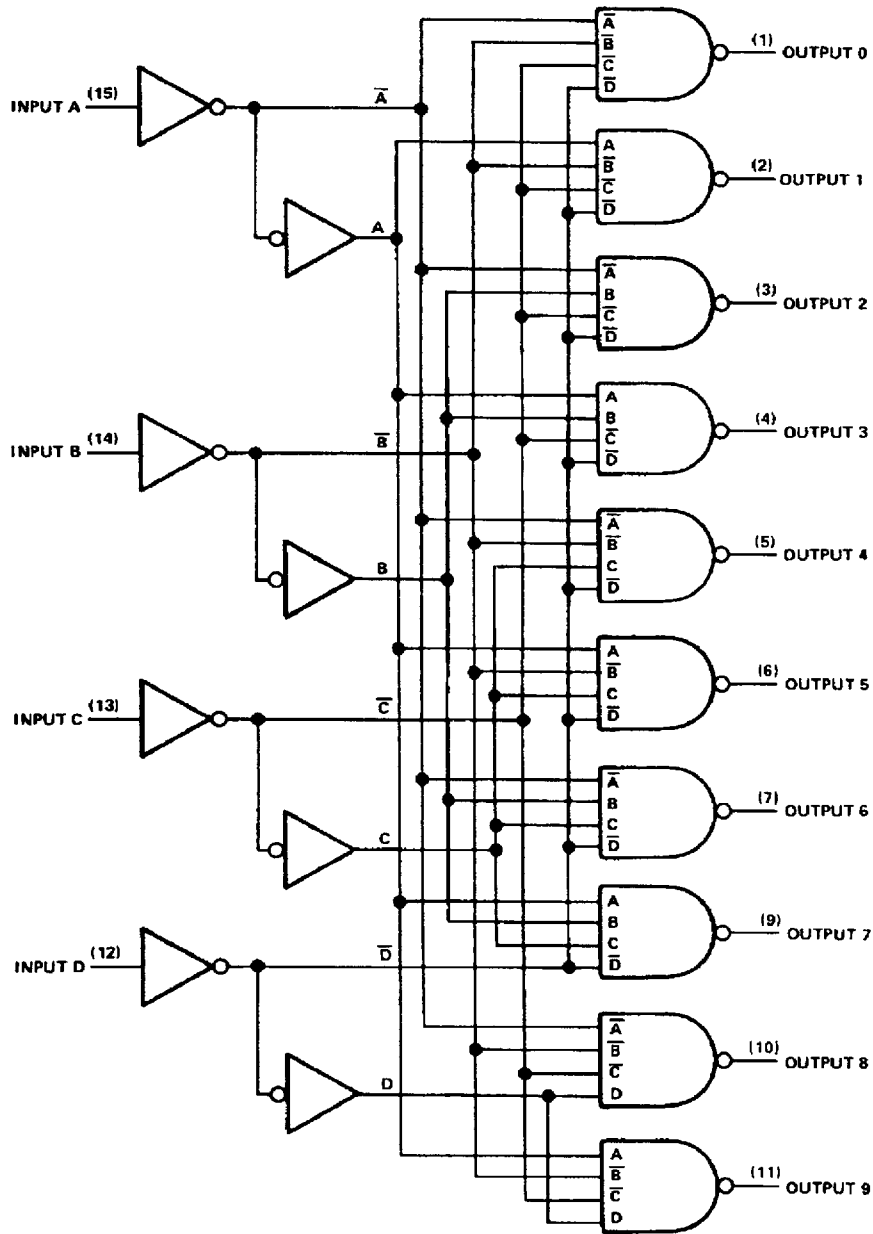
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TYPES SN5442A, SN54L42, SN54LS42, SN7442A, SN74LS42  
 4-LINE TO 10-LINE DECODERS (1-OF-10)

logic diagrams



Pin numbers shown on logic notation are for D, J or N packages

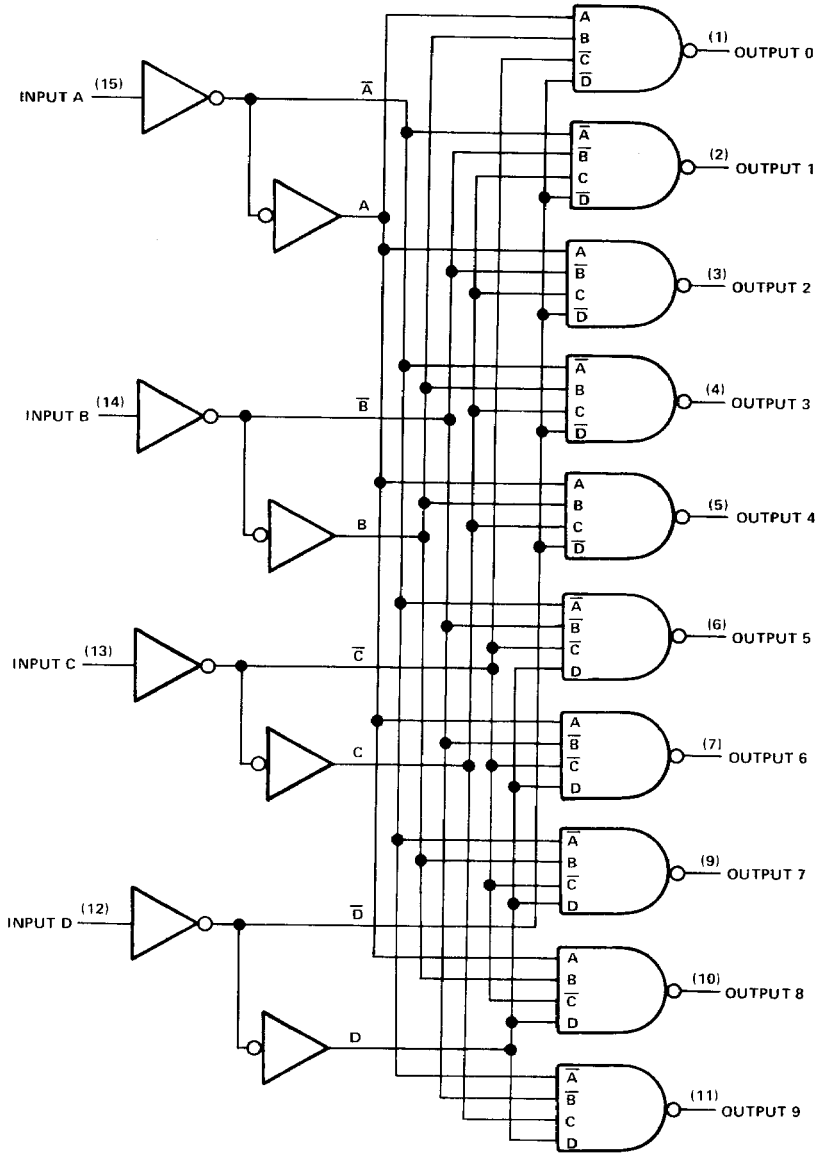
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TYPES SN5443A, SN54L43, SN7443A  
4-LINE TO 10-LINE DECODERS (1-OF-10)

logic diagrams (continued)



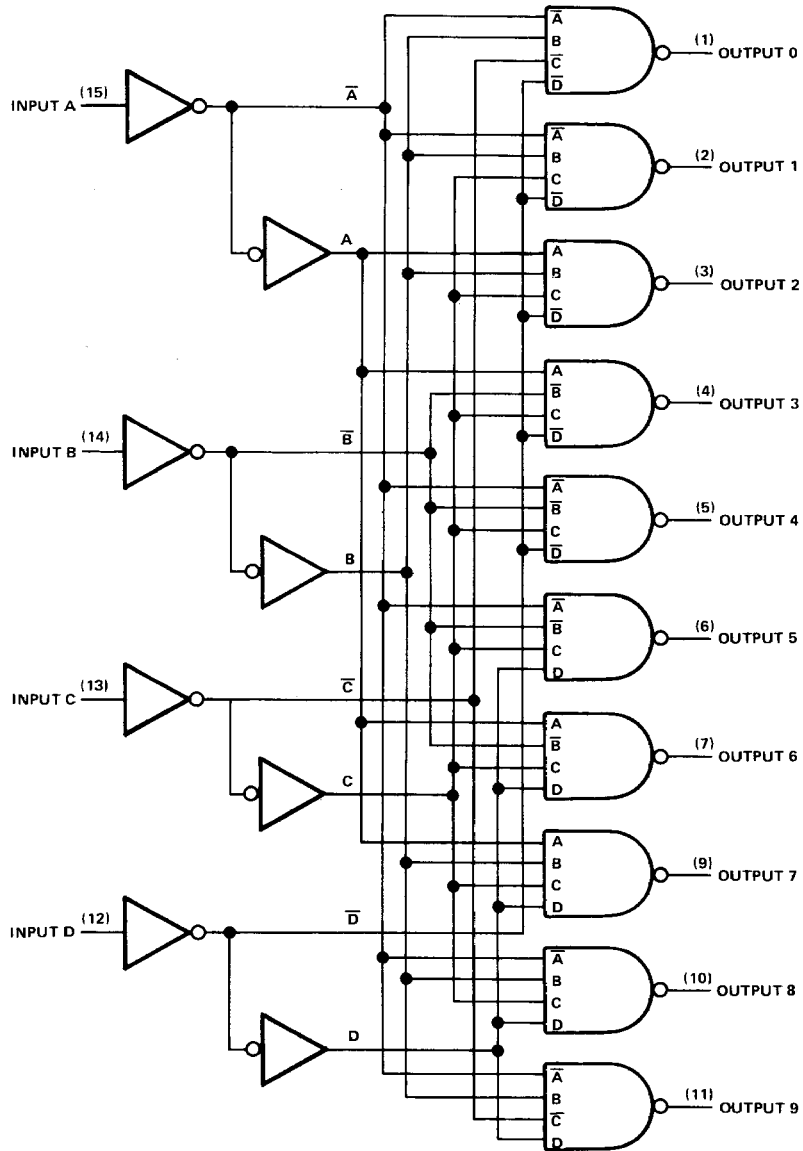
Pin numbers shown on logic notation are for D, J or N packages.

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TTL DEVICES

TYPES SN5444A, SN54L44, SN7444A  
4-LINE TO 10-LINE DECODERS (1-OF-10)

logic diagrams (continued)



Pin numbers shown on logic notation are for D, J or N packages.



TTL DEVICES

# TYPES SN54S195, SN74S195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range:	SN54S195 . . . . . $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
	SN74S195 . . . . . $0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN54S195			SN74S195			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-1	mA
Low-level output current, $I_{OL}$			20			20	mA
Clock frequency, $f_{clock}$	0		70	0		70	MHz
Width of clock input pulse, $t_w(\text{clock})$	7			7			ns
Width of clear input pulse, $t_w(\text{clear})$	12			12			ns
Setup time, $t_{SU}$ (see Figure 1)	Shift/load		11			11	ns
	Serial and parallel data		5			5	
	Clear inactive-state		9			9	
Shift/load release time, $t_{release}$ (see Figure 1)			6			6	ns
Serial and parallel data hold time, $t_h$ (see Figure 1)			3			3	ns
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}\text{C}$

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{IH}$ High-level input voltage			2			V
$V_{IL}$ Low-level input voltage					0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}$ ,	$I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ ,	$V_{IH} = 2 \text{ V}$ , $I_{OH} = -1 \text{ mA}$	SN54S195	2.5	3.4	V
			SN74S195	2.7	3.4	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}$ , $V_{IL} = 0.8 \text{ V}$ ,	$V_{IH} = 2 \text{ V}$ , $I_{OL} = 20 \text{ mA}$			0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}$ ,	$V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}$ ,	$V_I = 2.7 \text{ V}$			50	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}$ ,	$V_I = 0.5 \text{ V}$			-2	mA
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX}$		-40		-100	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}$ ,	See Note 2	SN54S195	70	99	mA
			SN74S195	70	109	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs,  $I_{CC}$  is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$f_{max}$ Maximum clock frequency	$C_L = 15 \text{ pF}$ , $R_L = 280 \Omega$ , See Figure 1	70	105		MHz	
$t_{PHL}$ Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns	
$t_{PLH}$ Propagation delay time, low-to-high-level output from clock				8	12	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from clock			11	16.5		ns

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TTL DEVICES



**TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44,  
SN54LS42, SN7442A THRU SN7444A, SN74LS42  
4-LINE TO 10-LINE DECODERS (1-OF-10)**

**FUNCTION TABLE**

NO.	'42A, 'L42, 'LS42 BCD INPUT				'43A, 'L43 EXCESS-3-INPUT				'44A, 'L44 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
	0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	L	L	H	H	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	L	H	L	L	L	H	H	H	L	H	H	H	H
5	L	H	L	H	H	L	L	L	L	H	H	L	L	L	H	H	H	H	L	H	H	H
6	L	H	H	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	L	H	H	L	L	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	L	L	L	H	L	H	L	L	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	L	L	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: '42A, '43A, '44A	5.5 V
'L42, 'L43, 'L44	5.5 V
'LS42	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

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**TTL DEVICES**

**TYPES SN5442A, SN5443A, SN5444A, SN7442A, SN7443A, SN7444A**  
**4-LINE TO 10-LINE DECODERS (1-OF-10)**

**recommended operating conditions**

	SN5442A SN5443A SN5444A			SN7442A SN7443A SN7444A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-800			-800	$\mu$ A
Low-level output current, $I_{OL}$			16			16	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN5442A SN5443A SN5444A		SN7442A SN7443A SN7444A		UNIT
		MIN	TYP‡	MAX	MIN	
$V_{IH}$ High-level input voltage		2		2		V
$V_{IL}$ Low-level input voltage				0.8		V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	1.5		-1.5		V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4	2.4	3.4	V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$	0.2 0.4		0.2 0.4		V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1		1		mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$	40		40		$\mu$ A
$I_{IL}$ Low level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	-1.6		-1.6		mA
$I_{OS}$ Short-circuit output current §	$V_{CC} = \text{MAX}$	-20	-55	-18	-55	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX},$ See Note 2	28	41	28	56	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 2:  $I_{CC}$  is measured with all outputs open and all inputs grounded.

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 3		14	25	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			17	30	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	25	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			17	30	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms

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**TTL DEVICES**

**TYPES SN54L42, SN54L43, SN54L44**  
**4-LINE TO 10-LINE DECODERS (1-OF-10)**

**recommended operating conditions**

	SN54L42 SN54L43 SN54L44			UNIT
	MIN	NOM	MAX	
V <sub>CC</sub> Supply voltage	4.5	5	5.5	V
V <sub>IH</sub> High-level input voltage	2			V
V <sub>IL</sub> Low-level input voltage			0.8	V
I <sub>OH</sub> High-level output current			-0.4	mA
I <sub>OL</sub> Low-level output current			8	mA
T <sub>A</sub> Operating free-air temperature	-55	125		°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = -12 mA			-1.5	V
V <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = -400 μA	2.4	3.4		V
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = 8 mA		0.2	0.4	V
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.8	mA
I <sub>OS</sub> §	V <sub>CC</sub> = MAX	-9		-28	mA
I <sub>CC</sub>	V <sub>CC</sub> = MAX, See Note 2		14	22	mA

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions. All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25° C.

§ Not more than one output should be shorted at a time.

NOTE 2: I<sub>CC</sub> is measured with all outputs open and inputs grounded.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25° C**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PHL</sub> Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 800 Ω, See Note 3	10	44	60	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic		46	70		ns
t <sub>PLH</sub> Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic		10	34	50	ns
t <sub>PLH</sub> Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic		52	70		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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**TTL DEVICES**



# TYPES SN54LS42, SN74LS42 4-LINE TO 10-LINE DECODERS (1-OF-10)

## recommended operating conditions

	SN54LS42			SN74LS42			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS42			SN74LS42			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IH}$ High-level input voltage		2			2			V
$V_{IL}$ Low-level input voltage				0.7			0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$			0.25	0.4	0.25	0.4	V
						0.35	0.5	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	$\mu$ A
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX}$			-20	-100	-20	-100	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$			7	13	7	13	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2.  $I_{CC}$  is measured with all outputs open and inputs grounded.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 3}$		15	25	ns
$t_{PHL}$ Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			20	30	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			15	25	ns
$t_{PLH}$ Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			20	30	ns

Note 3: See General Information Section for load circuits and voltage waveforms.

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