MOTOROLA

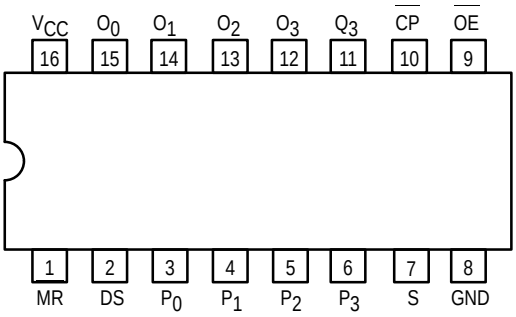
SN74LS395

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

The SN74LS395 is a 4-Bit Register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active HIGH Output Enable (OE) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

- Shift Left or Parallel 4-Bit Register
- 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



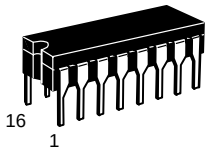
PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
D_S	Serial Data Input	0.5 U.L.	0.25 U.L.
$\overline{S}$	Mode Select Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
OE	Output Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
O_0-O_3	3-State Register Outputs	65 U.L.	15 U.L.
Q_3	Register Output	10 U.L.	5 U.L.

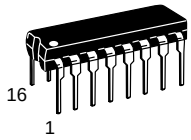
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

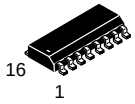
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

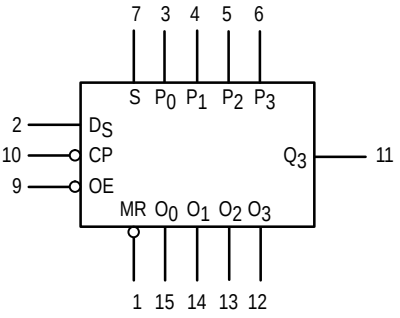


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

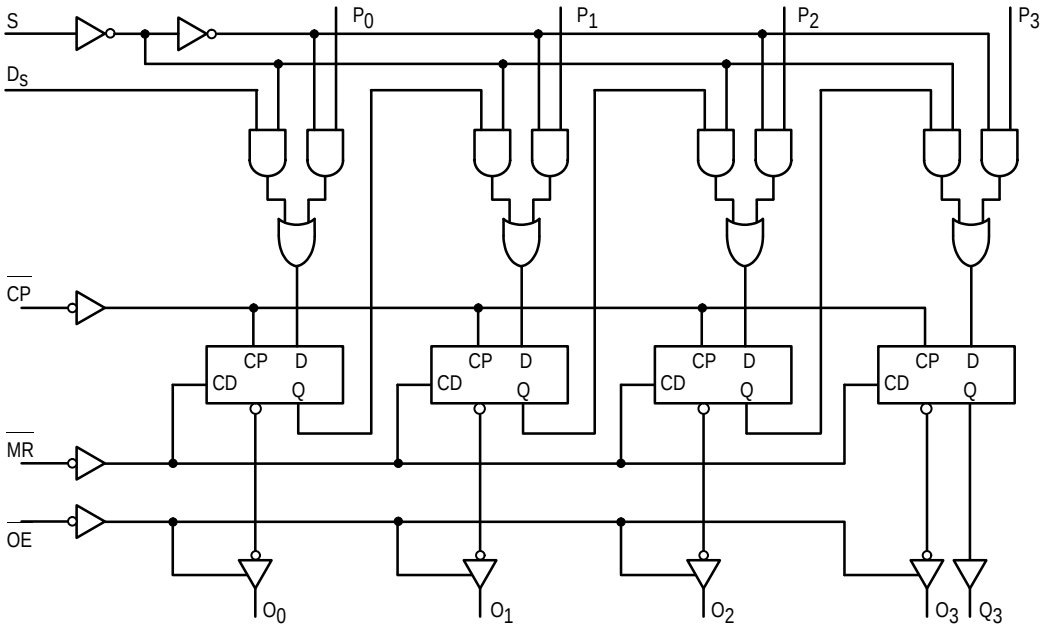
SN74LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



FUNCTION DESCRIPTION

The SN74LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel (P_n) input or from the preceding stage. When the Select input is HIGH, the P_n inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (CP) input. Signals on the P_n, D_S and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the S input is LOW, a CP HIGH-LOW transition transfers data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3. A left-shift is accomplished by connecting the outputs back to the P_n inputs, but offset one place to the left, i.e., O_3 to P_2, O_2 to P_1 and O_1 to P_0, with P_3 acting as the linking input from another package.

When the OE input is HIGH, the output buffers are disabled and the Q_0-Q_3 outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

MODE SELECT — TRUTH TABLE

Operating Mode	Inputs @ t_n					Outputs @ t_{n+1}			
	$\overline{MR}$	$\overline{CP}$	S	D_S	P_n	O_0	O_1	O_2	O_3
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H	↘	L	H	X	H	O_{0n}	O_{1n}	O_{2n}
Shift, RESET First Stage	H	↘	L	L	X	L	O_{0n}	O_{1n}	O_{2n}
Parallel Load	H	↘	H	X	P_n	P_0	P_1	P_2	P_3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

$t_{n,\ n+1}$ = time before and after CP HIGH-to-LOW transition

NOTE:
When OE is HIGH, outputs O_0-O_3 are in the high impedance state; however, this does not affect other operations or the Q_3 output.

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			−0.4	mA
I_{OL}	Output Current — Low			8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA
I_{OZH}	Output Off Current HIGH			20	μA	V_{CC} = MAX, V_O = 2.4 V
I_{OZL}	Output Off Current LOW			−20	μA	V_{CC} = MAX, V_O = 0.4 V
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
				−0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current (Note 1)	−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH			31	mA	V_{CC} = MAX, $\overline{OE}$ = GND, $\overline{CP}$ = GND
	Total, Output LOW			34	mA	V_{CC} = MAX, $\overline{OE}$ = 4.5 V, $\overline{CP}$ momentary 3.0 V then GND

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

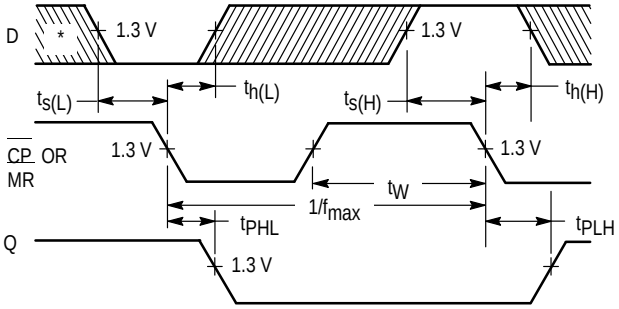
Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Propagation Delay, Clear to Output		22	35	ns	
t_{PLH} t_{PHL}	Propagation Delay, Low to High Propagation Delay, High to Low		15 25	30 30	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 17	25 25	ns	
t_{PLZ} t_{PHZ}	Output Disable Time		12 11	20 17	ns	C_L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_W	Clock Pulse Width	16			ns	V_{CC} = 5.0 V
t_s	Setup Time, Mode Select	40			ns	
t_s	Setup Time, All Others	20			ns	
t_h	Data Hold Time	10			ns	

AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



*The Data Input is D_S for S = LOW and P_n for S = HIGH.

Figure 1

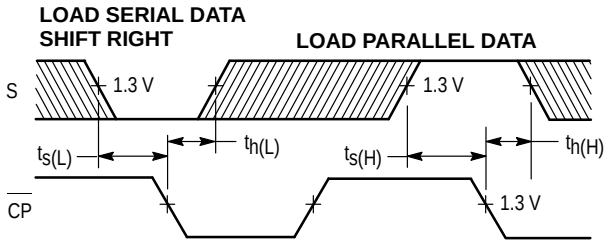


Figure 2

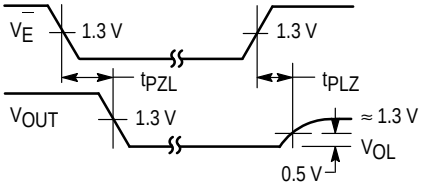


Figure 3

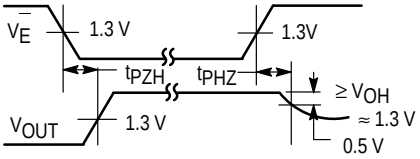
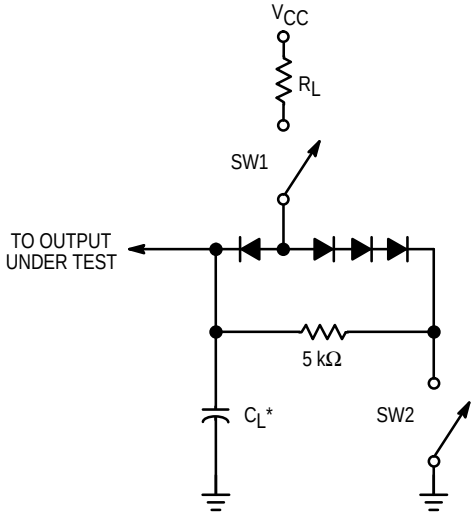


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 5

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed