

Synchronous Presettable 4-Bit Counter with Output Register (Multiplexed 3-State Outputs)

TC74HC691 Binary, Asynchronous clear

The TC74HC691A is a high speed CMOS COUNTER/REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It is a 4-BIT BINARY COUNTER.

If the LOAD input (LOAD) is held low, DATA input (A - D) are loaded in internal counter on the positive edge of the counter clock input (CCK). In counter mode, the internal counter counts up on the positive edge of counter clock. Counter clear input (CCLR) is active low. The counter clear is asynchronous.

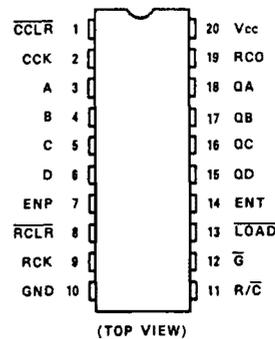
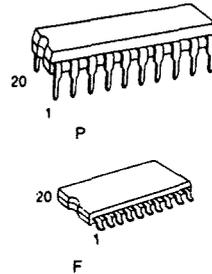
The internal counter's outputs are stored in the output register on the positive edge of register clock (RCK). Register clear (RCLR) is active low. The register clear function is asynchronous to RCK. At this point, internal counter outputs do not change. The outputs (QA - QD) are selected from the internal counter outputs or register outputs by output select (R/C).

Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of counters without using external gate.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

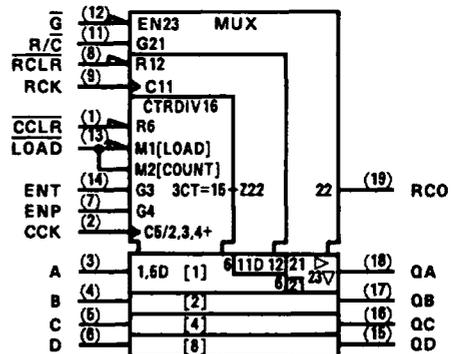
Features

- High Speed: $f_{MAX} = 63\text{MHz(Typ.)}$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A(Max.)}$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min)
- Output Drive Capability: 15 LSTTL Loads For QA ~ QH
10 LSTTL Loads For RCO
- Symmetrical Output Impedance: $I_{OH} = I_{OL} = 6\text{mA(Min.)}$
For QA ~ QH
 $I_{OH} = I_{OL} = 4\text{mA(Min.)}$
For RCO
- Balanced Propagation Delays: $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range: $V_{CC(opr)} = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS691



(TOP VIEW)

Pin Assignment



IEC Logic Symbol

Truth Table

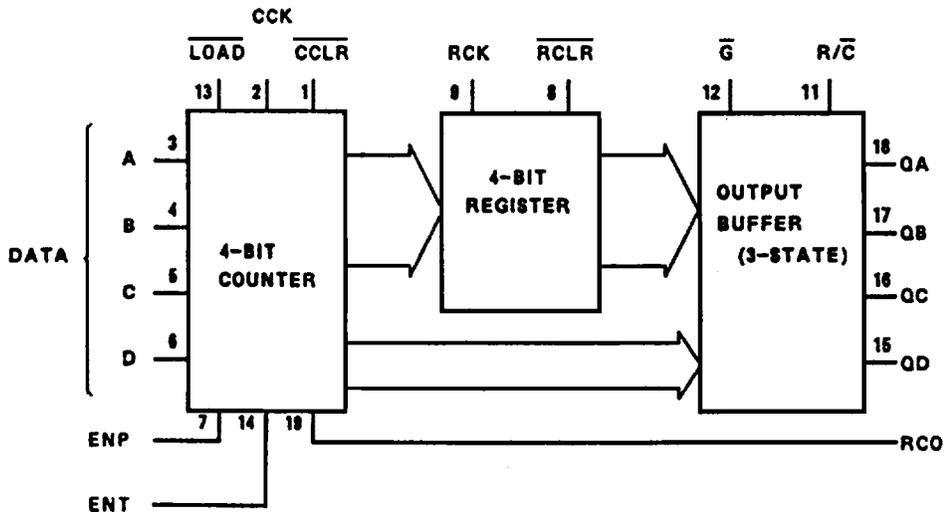
Inputs									Outputs				Function
CCLR	LOAD	ENP	ENT	RCLR	CCK	RCK	R/C	\bar{G}	QA	QB	QC	CD	
X	X	X	X	X	X	X	X	H	Z	Z	Z		High Impedance
L	X	X	X	X	X	X	L	L	L	L	L	L	Counter Clear
H	L	X	X	X	\int	X	L	L	a	b	c	d	Load Data
H	H	L	X	X	\int	X	L	L	No change			Count Disable No change	
H	H	X	L	X	\int	X	L	L	No change				
H	H	H	H	X	\int	X	L	L	Count up			Count up	
H	X	X	X	X	\int	X	L	L	No change			No count	
X	X	X	X	L	X	X	H	L	L	L	L	L	Register clear
X	X	X	X	H	X	\int	H	L	a'	b'	c'	d'	Load register
X	X	X	X	X	X	\int	G	L	No change			No change	

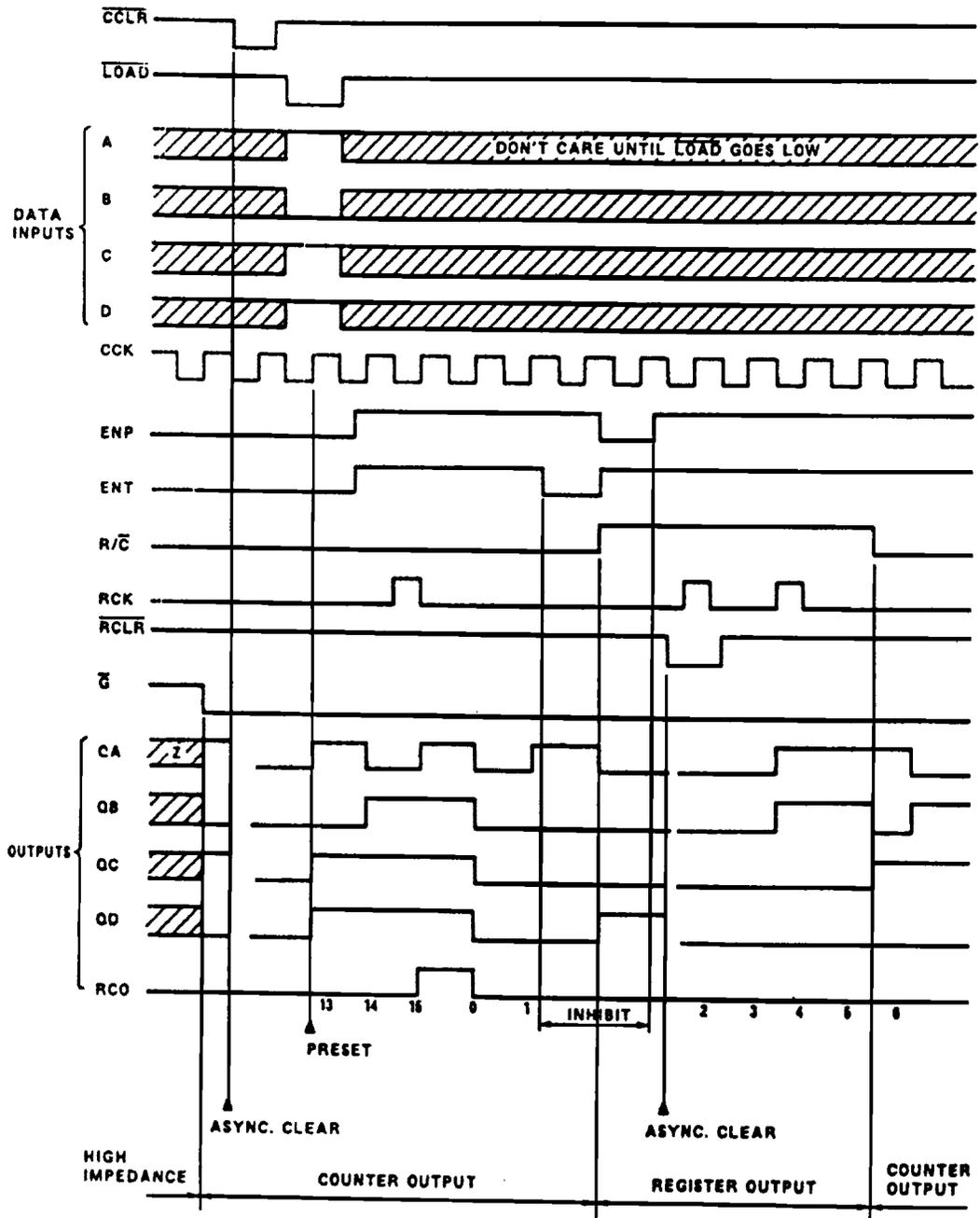
X : Don't Care

Z : High Impedance

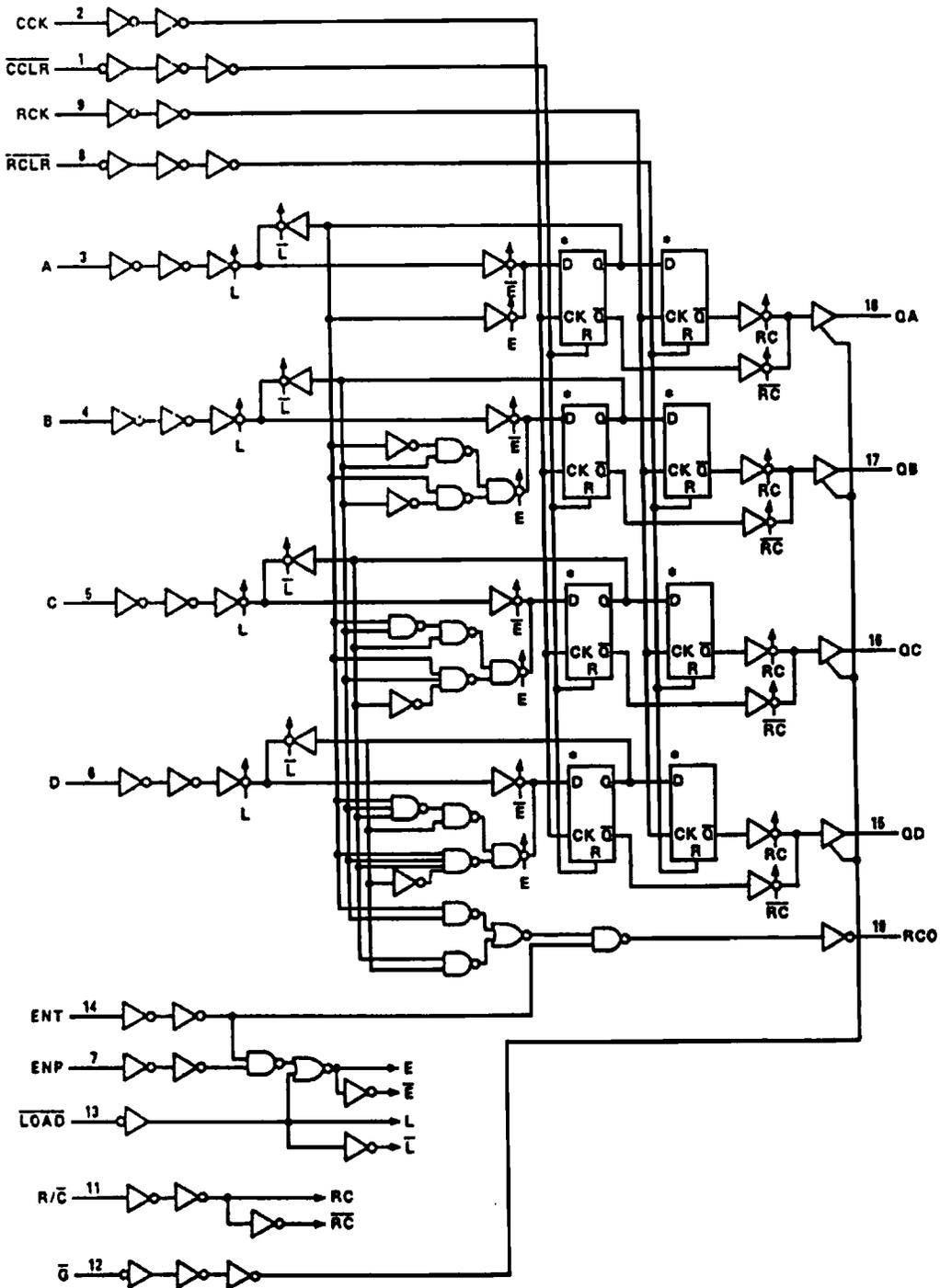
a - d: The level of steady state input voltage at inputs A- D respectively.

a' - d': The level of internal counter outputs respectively, before the most recent positive edge of the register clock.





Timing Chart



Logic Diagram

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 - 7	V
DC Input Voltage	V_{IN}	-0.5 - $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5 - $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current (RCO) ($Q_A - Q_H$)	I_{OUT}	± 25 ± 35	mA
DC V_{CC} /Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)* / 180(SOIC)	mW
Storage Temperature	T_{stg}	-65 - 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 - 6	V
Input Voltage	V_{IN}	0 - V_{CC}	V
Output Voltage	V_{OUT}	0 - V_{CC}	V
Operating Temperature	T_{opr}	-40 - 85	°C
Input Rise and Fall Time	t_r, t_f	0 - 1000($V_{CC} = 2.0\text{V}$) 0 - 500($V_{CC} = 4.5\text{V}$) 0 - 400($V_{CC} = 6.0\text{V}$)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		Unit	
				V_{CC}	Min.	Typ.	Max.	Min.		Max.
High-Level Input Voltage	V_{IH}	-		2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}	-		2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		RCO	$I_{OH} = -4\text{mA}$ $I_{OH} = -5.2\text{mA}$	4.5	4.18	4.31	-	4.13	-	
				6.0	5.68	5.80	-	5.63	-	
				6.0	5.68	5.80	-	5.63	-	
$Q_A - Q_H$	$I_{OH} = -6\text{mA}$ $I_{OH} = -7.8\text{mA}$	4.5	4.18	4.31	-	4.13	-			
		6.0	5.68	5.80	-	5.63	-			
		6.0	5.68	5.80	-	5.63	-			
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20\mu\text{A}$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		RCO	$I_{OH} = 4\text{mA}$ $I_{OH} = 5.2\text{mA}$	4.5	-	0.17	0.26	-	0.33	
				6.0	-	0.18	0.26	-	0.33	
				6.0	-	0.18	0.26	-	0.33	
$Q_A - Q_H$	$I_{OL} = 6\text{mA}$ $I_{OL} = 7.8\text{mA}$	4.5	-	0.17	0.26	-	0.33			
		6.0	-	0.18	0.26	-	0.33			
		6.0	-	0.18	0.26	-	0.33			
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	6.0	-	-	± 0.5	-	± 5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	± 0.1	-	± 1.0		
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	6.0	-	-	4.0	-	40.0		

Timing Requirements (Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V _{CC}	Typ.	Limit	Limit		
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	-	2.0	-	75	95		ns
			4.5	-	15	19		
			6.0	-	12	15		
Minimum Pulse Width (CCLR, RCLR)	$t_{W(L)}$	-	2.0	-	75	95		
			4.5	-	15	19		
			6.0	-	12	15		
Minimum Setup Time (CCLR, RCLR)	t_s	-	2.0	-	100	125		
			4.5	-	20	25		
			6.0	-	16	20		
Minimum Setup Time (LOAD, ENT, ENP)	t_s	-	2.0	-	150	190		
			4.5	-	30	38		
			6.0	-	24	25		
Minimum Setup Time (A, B, C, D)	t_s	-	2.0	-	125	155		
			4.5	-	25	31		
			6.0	-	20	25		
Minimum Setup Time (CCK-RCK)	t_s	-	2.0	-	125	155		
			4.5	-	25	31		
			6.0	-	20	25		
Minimum Hold Time	t_h	-	2.0	-	0	0		
			4.5	-	0	0		
			6.0	-	0	0		
Minimum Removal Time	t_{rem}	-	2.0	-	50	65		
			4.5	-	10	13		
			6.0	-	8	10		
Clock Frequency	f	-	2.0	-	4	3.5		MHz
			4.5	-	22	18		
			6.0	-	26	21		

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time (RCO)	t_{TLH} t_{THL}	-	-	4	8	ns
Propagation Delay Time (CCK-RCO)	t_{pLH} t_{pHL}	-	-	18	32	
Propagation Delay Time (ENT-RCO)	t_{pLH} t_{pHL}	-	-	8	15	
Propagation Delay Time (CCLR-RCO)	t_{pLH}	-	-	19	34	
Maximum Clock Frequency	f_{MAX}	-	24	63	-	MHz

AC Electrical Characteristics ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit	
			CL	V _{CC}	Min.	Typ.	Max.		Min.
Output Transition Time (Q)	t_{TLH} t_{THL}	-	50	2.0	-	25	60	-	75
				4.5	-	7	12	-	15
				6.0	-	6	10	-	13
Output Transition Time (RCO)	t_{TLH} t_{THL}	-	50	2.0	-	30	75	-	95
				4.5	-	8	15	-	19
				6.0	-	7	13	-	16
Propagation Delay Time (CCK-Q)	t_{PLH}	-	50	2.0	-	84	215	-	270
				4.5	-	27	43	-	54
				6.0	-	22	34	-	43
	t_{PHL}	-	150	2.0	-	99	225	-	320
				4.5	-	32	51	-	64
				6.0	-	26	41	-	51
Propagation Delay Time (RCK-Q)	t_{PLH}	-	50	2.0	-	84	215	-	270
				4.5	-	28	43	-	54
				6.0	-	22	34	-	43
	t_{PHL}	-	150	2.0	-	99	225	-	320
				4.5	-	33	51	-	64
				6.0	-	26	41	-	51
Propagation Delay Time (R/C-Q)	t_{PLH}	-	50	2.0	-	63	170	-	215
				4.5	-	21	34	-	43
				6.0	-	17	27	-	34
	t_{PHL}	-	150	2.0	-	78	210	-	265
				4.5	-	26	42	-	53
				6.0	-	21	34	-	42
Propagation Delay Time (CCLR-Q)	t_{PHL}	-	50	2.0	-	93	250	-	315
				4.5	-	31	50	-	63
				6.0	-	25	40	-	50
			150	2.0	-	108	290	-	365
				4.5	-	36	58	-	73
				6.0	-	29	46	-	58
Propagation Delay Time (RCLR-Q)	t_{PHL}	-	50	2.0	-	90	250	-	315
				4.5	-	30	50	-	63
				6.0	-	24	40	-	50
			150	2.0	-	105	290	-	365
				4.5	-	35	58	-	73
				6.0	-	28	46	-	58
Propagation Delay Time (CCK-RCO)	t_{PLH} t_{PHL}	-	50	2.0	-	72	185	-	230
				4.5	-	23	37	-	46
				6.0	-	19	30	-	37
Propagation Delay Time (ENT-RCO)	t_{PLH} t_{PHL}	-	50	2.0	-	36	95	-	120
				4.5	-	12	19	-	24
				6.0	-	10	15	-	19
Propagation Delay Time (CCLR-RCO)	t_{PHL}	-	50	2.0	-	75	195	-	245
				4.5	-	25	39	-	49
				6.0	-	20	31	-	39
Output Enable Time (G-Q)	t_{GZL}	$R_L = 1\text{k}\Omega$	50	2.0	-	48	120	-	150
				4.5	-	16	24	-	30
				6.0	-	13	19	-	24
	t_{GZH}		150	2.0	-	63	160	-	200
				4.5	-	21	32	-	40
				6.0	-	17	26	-	32
Output Disable Time (G-Q)	t_{GZL} t_{GZH}	$R_L = 1\text{k}\Omega$	50	2.0	-	34	145	-	180
				4.5	-	18	29	-	36
				6.0	-	14	23	-	29

ns

AC Electrical Characteristics ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

Parameter	Symbol	Test Condition	Ta = 25°C			Ta = -40 ~ 85°C		Unit		
			CL	V _{CC}	Min.	Typ.	Max.		Min.	Max.
Maximum Clock Frequency	f _{MAX}	-	50	2.0	4	17	-	3.5	-	MHz
				4.5	22	52	-	18	-	
				6.0	26	65	-	21	-	
Input Capacitance	C _{IN}	-	-	-	5	10	-	10	pF	
Output Capacitance	C _{OUT}	-	-	-	13	-	-	-		
Power Dissipation Capacitance	C _{PD(1)}	-	-	-	63	-	-	-		

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$