TEXAS INSTRUMENTS

SN74LS292, SN74LS294

SDLS153A – JANUARY 1981 – REVISED JANUARY 2016

SN74LS29x Programmable Frequency Dividers and Digital Timers

1 Features

- Count Divider Chain
- Digitally Programmable from 2^2 to 2^n (n = 31 for SN74LS292 , n = 15 for SN74LS294)
- Useable Frequency Range from DC to 30 MHz
- Easily Expandable

2 Applications

- Frequency Division
- Digital Timing

3 Description

The SN74LS29x devices are programmable frequency dividers and digital timers contain 31 flip-flops plus 30 gates (in SN74LS292) or 15 flip-flops plus 29 gates (in SN74LS294) on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low $\overline{CLR}$ clear input to initialize the state of all flip-flops. To facilitate the incoming inspection, test points are provided (TP1, TP2, and TP3 on the SN74LS292, and TP on the SN74LS294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating (see Table 1).

A brief look at the digital timing capabilities of the SN74LS292 shows that with a 1-MHz input frequency, programming for 2^{10} gives a period of 1.024 ms, 2^{20} gives a period of 1.05 sec, 2^{26} gives a period of 1.12 min, and 2^{31} gives a period of 35.79 min.

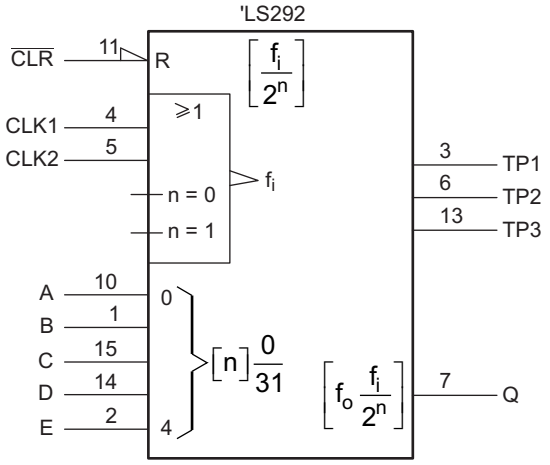
These devices are easily cascadable, giving limitless possibilities to achievable timing delays.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LS292N	PDIP (16)	6.35 mm × 19.30 mm
SN74LS294N		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Symbols



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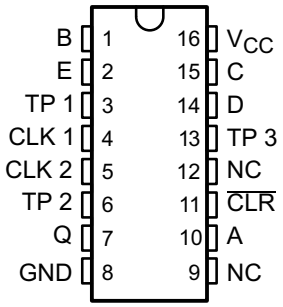
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 1981) to Revision A	Page
• Removed SN54LS292 and SN54LS294 from the data sheet	1
• Added *ESD Ratings* and *Thermal Information* tables, *Feature Description* section, *Device Functional Modes* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

SN74LS29x J, W, or N Package
16-Pin PDIP
Top View



Pin Functions, SN74LS292

PIN		I/O	DESCRIPTION
NAME	PDIP		
A	10	I	Programming input A
B	1	I	Programming input B
C	15	I	Programming input C
CLK1	4	I	Clock 1 input
CLK2	5	I	Clock 2 input
$\overline{CLR}$	11	I	Active-low clear input
D	14	I	Programming input D
E	2	I	Programming input E
GND	8	-	Ground
NC	9, 12	-	No connect
Q	7	O	Q Output
TP	—	O	Test Point
TP1	3	O	Test Point
TP2	6	O	Test Point
TP3	13	O	Test Point
V_{CC}	16	-	Power

Pin Functions, SN74LS294

PIN		I/O	DESCRIPTION
NAME	PDIP		
A	2	I	Programming input A
B	1	I	Programming input B
C	15	I	Programming input C
CLK1	4	I	Clock 1 input
CLK2	5	I	Clock 2 input
$\overline{CLR}$	11	I	Active-low clear input
D	14	I	Programming input D
E	—	I	Programming input E
GND	8	-	Ground
NC	6, 9 ,10, 12, 13	-	No connect
Q	7	O	Q Output
TP	3	O	Test Point
TP1	—	O	Test Point
TP2	—	O	Test Point
TP3	—	O	Test Point
V_{CC}	16	-	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}(2)	Supply voltage		7	V
	Input voltage		7	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network ground terminal.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current (Q only)				–1.2	mA
I_{OL}	Low-level output current (Q only)				24	mA
f_{clock}	Clock frequency		0		30	MHz
t_w	Duration of clock input pulse		16			ns
t_w	Duration of clear pulse	SN74LS292	55			ns
		SN74LS294	35			
t_{su}	Clear inactive-state set-up time		15			ns
T_A	Operating free-air temperature		0		70	°C

6.3 Thermal Information

THERMAL METRIC[1]		SN74LS292 N (PDIP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = MIN, I_I = –18 mA				–1.5	V
V_{OH}	Q	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = –1.2 mA, V_{IL} = MAX		2.4	3.4		V
V_{OL}	Q	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4	V
			I_{OL} = 24 mA		0.35	0.5	
	TP[3]		I_{OL} = 0.5 mA		0.25	0.4	
I_I		V_{CC} = MAX, V_I = 7 V				0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				20	mA
I_{IL}	CLK1, CLK2	V_{CC} = MAX, V_I = 0.4 V				–0.8	mA
	All others	V_{CC} = MAX, V_I = 0.4 V				–0.4	
I_{OS}[4]	Q	V_{CC} = MAX		–30		–130	mA
I_{CC}	SN74LS292	V_{CC} = MAX, all inputs grounded, all outputs open			40	75	mA
	SN74LS294	V_{CC} = MAX, all inputs grounded, all outputs open			30	50	

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Recommended Operating Conditions*.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(3) The TP output or outputs are not intended to drive external loads, but are solely provided for test points.
(4) The duration of the short-circuit should not exceed one second.

6.5 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C, R_L = 667 Ω, C_L = 45 pF (see Figure 1)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	From CLK1 or 2		30	50		MHz
t_{PLH}	From CLK1 or 2, to Q; Modulo set at 2^2, A through # = LLLHL (xxxxLS292), A through D = LLHL (xxxxLS294)			55	90	ns
t_{PHL}	From CLK1 or 2, to Q; Modulo set at 2^2, A through # = LLLHL (xxxxLS292), A through D = LLHL (xxxxLS294)			80	120	ns
	From $\overline{CLR}$, to Q	SN74LS292		85	130	
		SN74LS294		35	65	

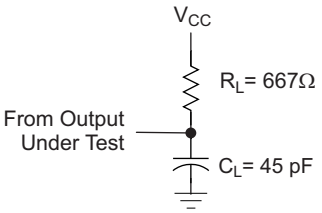


Figure 1. Switching Loads

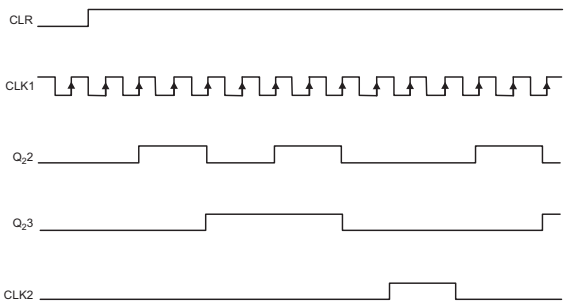


Figure 2. Timing Diagram

6.6 Typical Characteristics

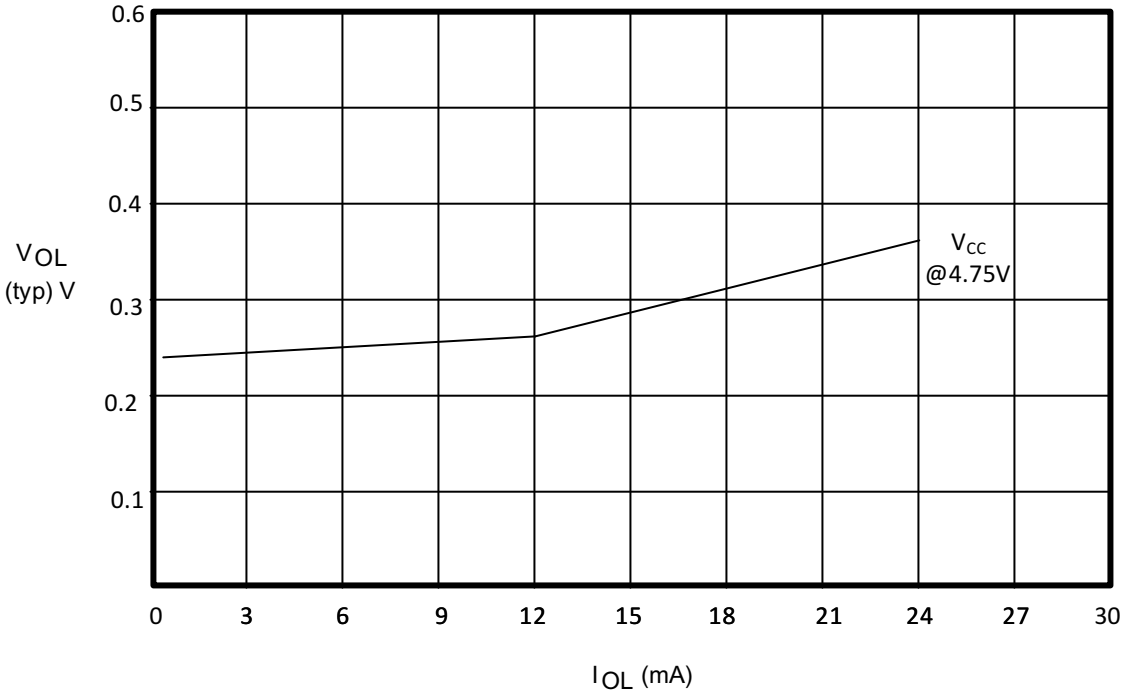
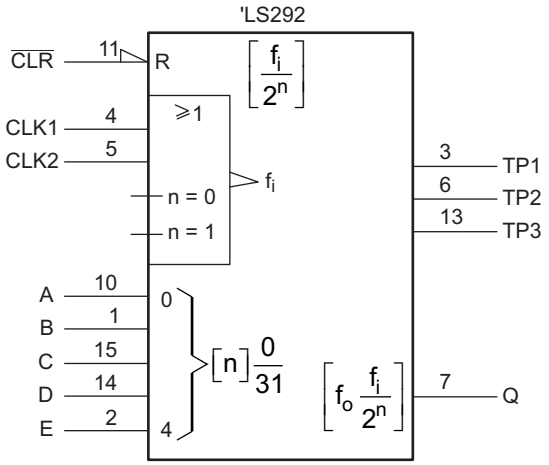


Figure 3. V_{OL} vs I_{OL}

7 Parameter Measurement Information

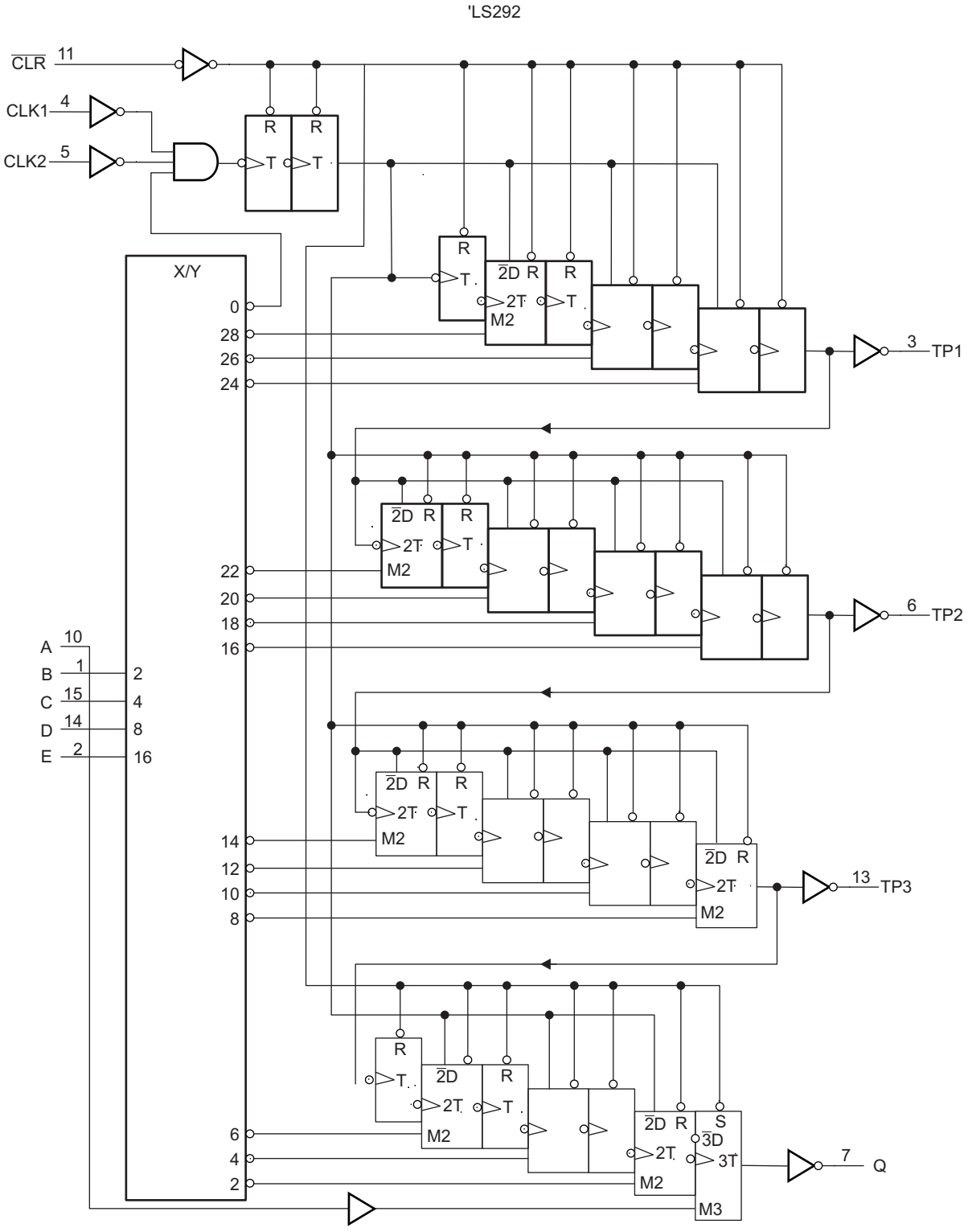
7.1 Logic Diagrams



These symbols are in accordance with ANSi/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

Figure 4. Logic Symbols

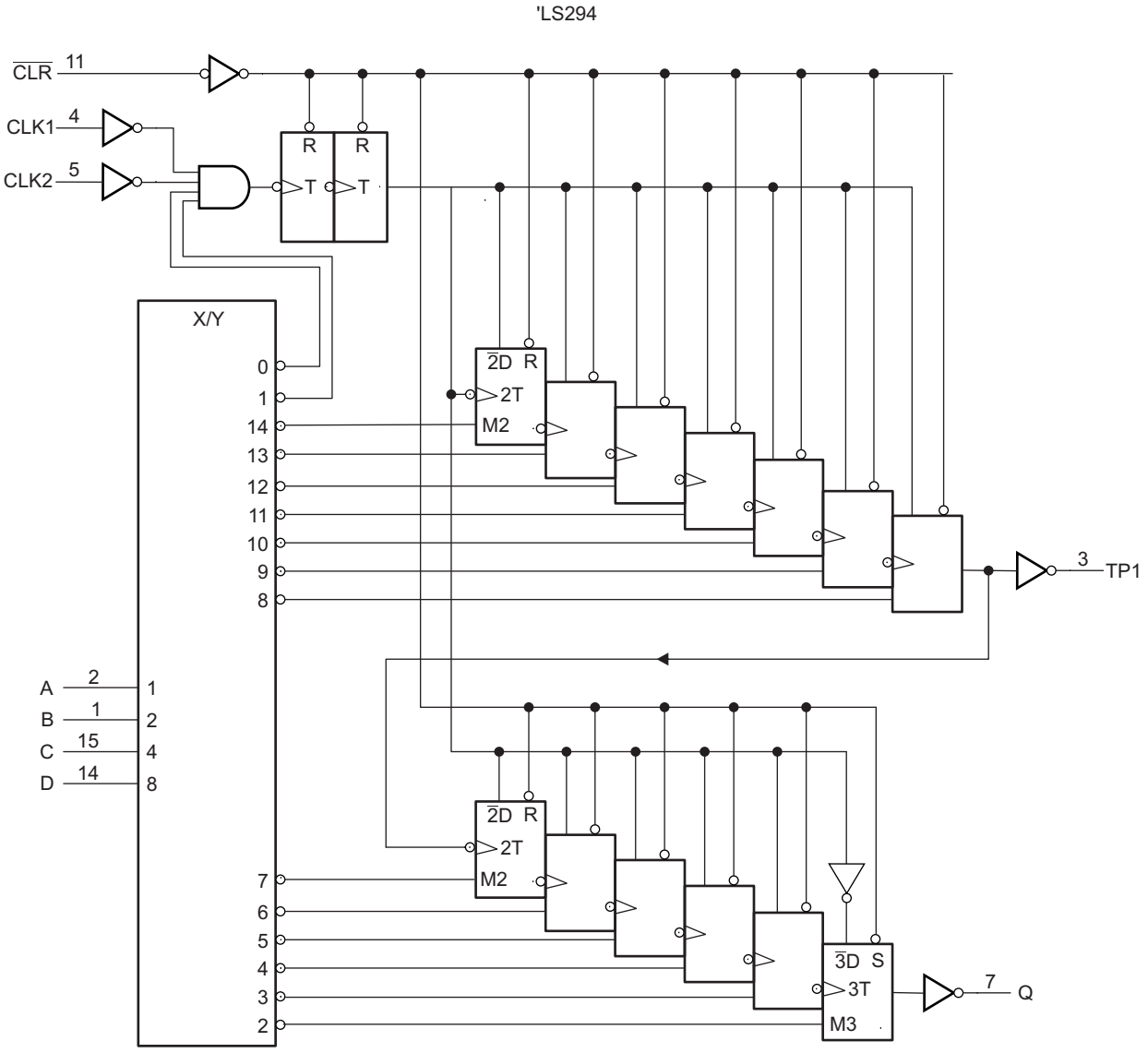
Logic Diagrams (continued)



Pin numbers shown are for J, N, and W packages.

Figure 5. Logic Diagram (Positive Logic) SN74LS292

Logic Diagrams (continued)



Pin numbers shown are for J, N, and W packages.

Figure 6. Logic Diagram (Positive Logic) SN74LS294

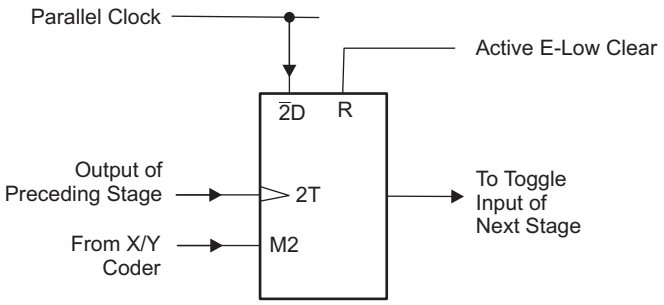
8 Detailed Description

8.1 Overview

Functional Block Diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode control inputs of several flip-flops. These flip-flops with mode controls each have a D input connected to the parallel clock line, and a T input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

The X/Y decoder output selected by the programming inputs goes low. While a mode control is slow, the D input of that flip-flop is enabled, and the signal from the parallel clock line ($f_{in} \div 4$) is passed to the T input of the following stage. All the other mode controls are high, enabling the T inputs and causing each flip-flop in turn to divide by two.

8.2 Functional Block Diagram



8.3 Feature Description

This SN74LS29x device can be used to digitally program from 2^2 to 2^n (n = 31 for SN74LS292, n = 15 for SN74LS294) divider chain. This has a useable frequency range up to 30 MHz. The flexibility is offered when the devices are cascaded to have desired timing delay.

8.4 Device Functional Modes

Table 1, Table 2, and Table 3 list the functional modes of the SN74LS292.

Table 1. Function Table

CLEAR	CLK1	CLK2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

Table 2. SN74LS292 Function Table

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131072	2^{24}	16777216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131072	2^{24}	16777216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131072	2^{24}	16777216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131072	2^{24}	16777216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131072	2^{24}	16777216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131072	2^{24}	16777216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131072	2^2	4
L	H	L	H	L	2^{10}	1024	2^9	512	2^{17}	131072	2^4	16
L	H	L	H	H	2^{11}	2048	2^9	512	2^{17}	131072	2^4	16
L	H	H	L	L	2^{12}	4096	2^9	512	2^{17}	131072	2^6	64
L	H	H	L	H	2^{13}	8192	2^9	512	2^{17}	131072	2^6	64
L	H	H	H	L	2^{14}	16384	2^9	512	Disabled low	Disabled low	2^8	256
L	H	H	H	H	2^{15}	32768	2^9	512	Disabled low	Disabled low	2^8	256
H	L	L	L	L	2^{16}	65536	2^9	512	2^3	8	2^{10}	1024
H	L	L	L	H	2^{17}	131072	2^9	512	2^3	8	2^{10}	1024
H	L	L	H	L	2^{18}	262144	2^9	512	2^5	32	2^{12}	4096
H	L	L	H	H	2^{19}	524288	2^9	512	2^5	32	2^{12}	4096
H	L	H	L	L	2^{20}	1048576	2^9	512	2^7	128	2^{14}	16384
H	L	H	L	H	2^{21}	2097152	2^9	512	2^7	128	2^{14}	16384
H	L	H	H	L	2^{22}	4194304	Disabled low	Disabled low	2^9	512	2^{16}	65536
H	L	H	H	H	2^{23}	8388608	Disabled low	Disabled low	2^9	512	2^{16}	65536
H	H	L	L	L	2^{24}	16777216	2^3	8	2^{11}	2048	2^{18}	262144
H	H	L	L	H	2^{25}	33554432	2^3	8	2^{11}	2048	2^{18}	262144
H	H	L	H	L	2^{26}	67108864	2^5	32	2^{13}	8192	2^{20}	1048576
H	H	L	H	H	2^{27}	134217728	2^5	32	2^{13}	8192	2^{20}	1048576
H	H	H	L	L	2^{28}	268435456	2^7	128	2^{15}	32768	2^{22}	4194304
H	H	H	L	H	2^{29}	536870912	2^7	128	2^{15}	32768	2^{22}	4194304
H	H	H	H	L	2^{30}	1073741824	2^9	512	2^{17}	131072	2^{24}	16777216
H	H	H	H	H	2^{31}	2147483648	2^9	512	2^{17}	131072	2^{24}	16777216

Table 3. SN74LS294 Function Table

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1024	2^4	16
H	L	H	H	2^{11}	2048	2^5	32
H	H	L	L	2^{12}	4096	2^6	64
H	H	L	H	2^{13}	8192	2^7	128
H	H	H	L	2^{14}	16384	2^8	256
H	H	H	H	2^{15}	32768	2^9	512

Figure 7, Figure 9, and Figure 9 show the schematics of inputs and outputs of the SN74LS292.

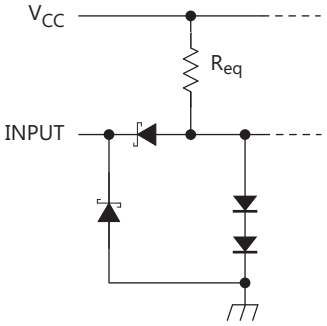


Figure 7. Equivalent of Each Input

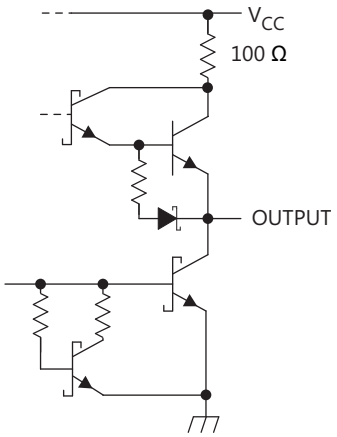


Figure 8. Typical of Q Outputs

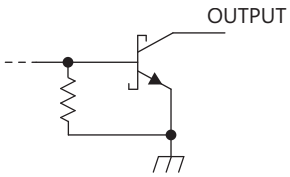


Figure 9. Typical of TP Outputs

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This device is used for configurable frequency, programmable frequency, and timing division as shown in *Typical Application*.

9.2 Typical Application

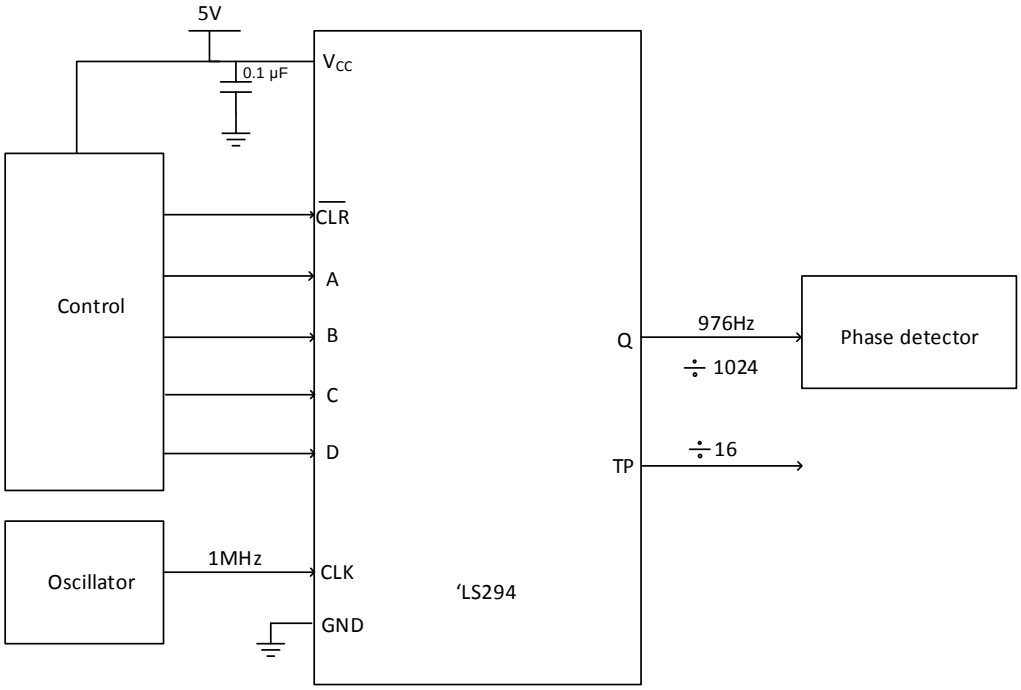


Figure 10. Typical application

9.2.1 Design Requirements

This device does not have balanced output drive. Take care to avoid bus contention because it can sink currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - Rise time and fall time specs. See (Δt/ΔV) in *Recommended Operating Conditions*.
   - Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
   - Inputs can go as high as (V_I max) in *Recommended Operating Conditions* at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed (I_{OH},I_{OL}) per output. These limits are located in the *Recommended Operating Conditions*.

Typical Application (continued)

9.2.3 Application Curve

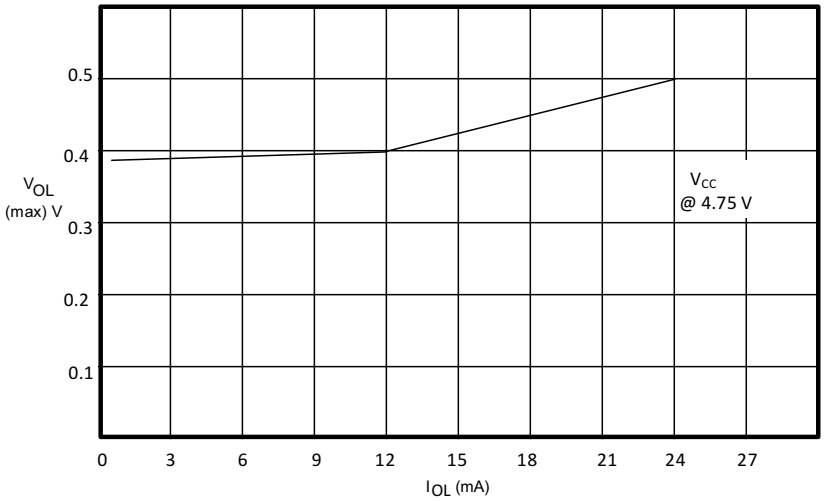


Figure 11. V_{OL} vs I_{OL}

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended and, if there are multiple V_{CC} pins, then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

The following are the rules that must be observed under all circumstances:

- All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating.
- The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever make more sense or is more convenient.

11.2 Layout Example

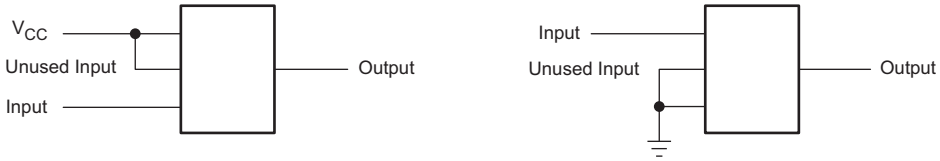


Figure 12. Generic Layout Best Practices

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Digital Phase-Locked Loop Design Using SN74LS297*, SDLA005
- *Introduction to Logic*, SLVA700

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LS292	Click here	Click here	Click here	Click here	Click here
SN74LS294	Click here	Click here	Click here	Click here	Click here

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.4 Trademarks

E2E is a trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS292N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS292N	Samples
SN74LS294N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS294N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

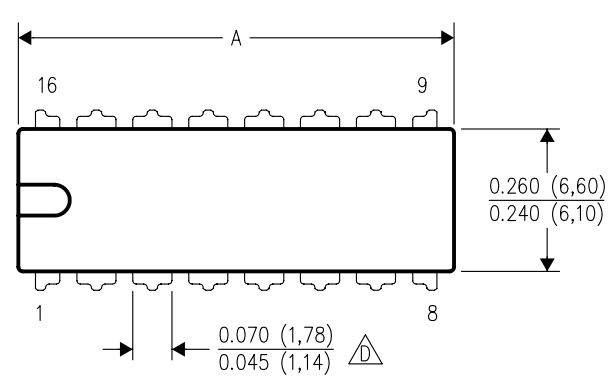
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

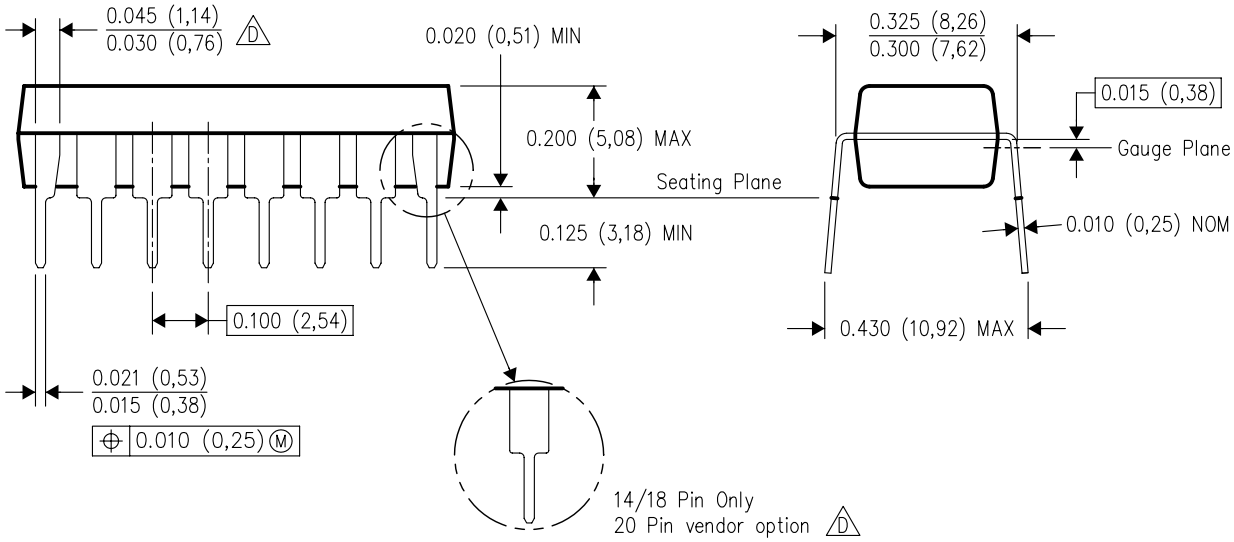
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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