



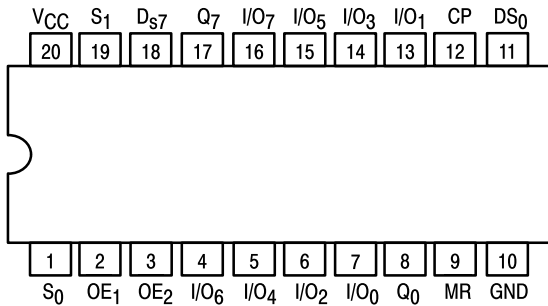
8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

The SN54/74LS299 is an 8-Bit Universal Shift/Storage Register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data.

The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q₀ and Q₇ to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

- Common I/O for Reduced Pin Count
- Four Operation Modes: Shift Left, Shift Right, Load and Store
- Separate Shift Right Serial Input and Shift Left Serial Input for Easy Cascading
- 3-State Outputs for Bus Oriented Applications
- Input Clamp Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)

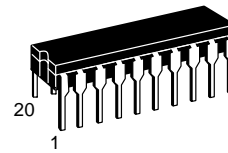


NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

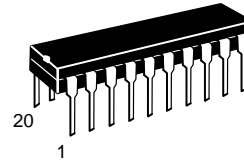
SN54/74LS299

8-BIT SHIFT/STORAGE REGISTER WITH 3-STATE OUTPUTS

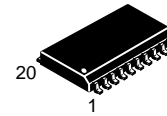
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

PIN NAMES

CP	Clock Pulse (active positive-going edge) Input
DS0	Serial Data Input for Right Shift
DS7	Serial Data Input for Left Shift
I/O _n	Parallel Data Input or Parallel Output (3-State) (Note c)
OE ₁ , OE ₂	3-State Output Enable (active LOW) Inputs
Q ₀ , Q ₇	Serial Outputs (Note b)
MR	Asynchronous Master Reset (active LOW) Input
S ₀ , S ₁	Mode Select Inputs

NOTES:

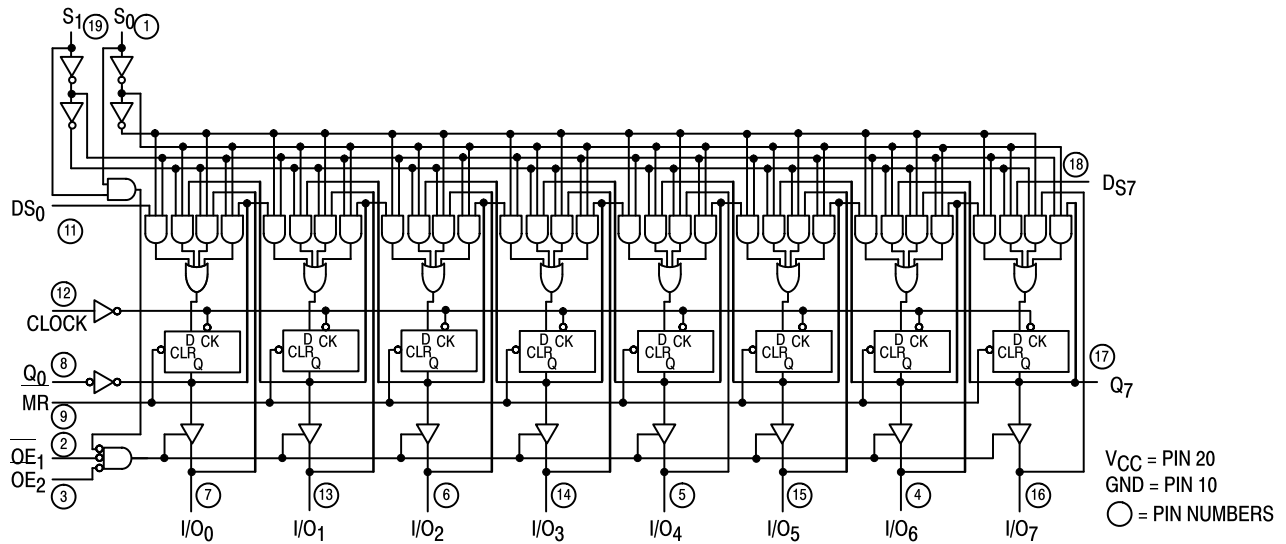
- 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.
- The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74). The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 (25) U.L.	15 (7.5) U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.
0.5 U.L.	0.25 U.L.
1 U.L.	0.5 U.L.

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								RESPONSE
MR	S ₁	S ₀	OE ₁	OE ₂	CP	DS ₀	DS ₇	
L	X	X	H	X	X	X	X	Asynchronous Reset; Q ₀ = Q ₇ = LOW I/O Voltage Undetermined
L	X	X	X	H	X	X	X	Asynchronous Reset; Q ₀ = Q ₇ = LOW I/O Voltage LOW
L	H	H	X	X	X	X	X	
L	L	X	L	L	X	X	X	Shift Right; D Q ₀ ; Q ₀ Q ₁ ; etc. Shift Right; D Q ₀ & I/O ₀ ; Q ₀ Q ₁ & I/O ₁ ; etc.
H	L	H	X	X	⌋	D	X	
H	L	H	L	L	⌋	D	X	Shift Left; D Q ₇ ; Q ₇ Q ₆ ; etc. Shift Left; D Q ₇ & I/O ₇ ; Q ₇ Q ₆ & I/O ₆ ; etc.
H	H	L	X	X	⌋	X	D	
H	H	L	L	L	⌋	X	D	Parallel Load; I/O _n Q _n
H	H	H	X	X	⌋	X	X	
H	L	L	H	X	X	X	X	Hold: I/O Voltage undetermined
H	L	L	X	H	X	X	X	
H	L	L	L	L	X	X	X	Hold: I/O _n = Q _n

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	Q ₀ , Q ₇	54, 74		-0.4	mA
I _{OL}	Output Current — Low	Q ₀ , Q ₇	54		4.0	mA
		Q ₀ , Q ₇	74		8.0	
I _{OH}	Output Current — High	I/O ₀ —I/O ₇	54		-1.0	mA
		I/O ₀ —I/O ₇	74		-2.6	
I _{OL}	Output Current — Low	I/O ₀ —I/O ₇	54		12	mA
		I/O ₀ —I/O ₇	74		24	

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage I/O ₀ -I/O ₇	54	2.4	3.2		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.4	3.1		V		
V _{OH}	Output HIGH Voltage Q ₀ , Q ₇	54	2.5	3.4		V	V _{CC} = MIN, I _{OH} = MAX	
		74	2.7	3.4		V		
V _{OL}	Output LOW Voltage I/O ₀ -I/O ₇	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
V _{OL}	Output LOW Voltage I/O ₀ -I/O ₇	54, 74			0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74			0.5	V	I _{OL} = 8.0 mA	
I _{OZH}	Output Off Current HIGH I/O ₀ -I/O ₇				40	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW I/O ₀ -I/O ₇				-400	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current	Others			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		S ₀ , S ₁ , I/O ₀ -I/O ₇			40	μA		
		Others			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
		S ₀ , S ₁ I/O ₀ -I/O ₇			0.2	mA		
I _{IL}	Input LOW Current	Others			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		S ₀ , S ₁			-0.8	mA		
I _{OS}	Short Circuit Current (Note 1)	Q ₀ , Q ₇	-20		-100	mA	V _{CC} = MAX	
		I/O ₀ -I/O ₇	-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				53	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

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AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency	25	35		MHz	C _L = 15 pF
t _{PHL} t _{PLH}	Propagation Delay, Clock to Q ₀ or Q ₇		26 22	39 33	ns	
t _{PHL}	Propagation Delay, Clear to Q ₀ or Q ₇		27	40	ns	
t _{PHL} t _{PLH}	Propagation Delay, Clock to I/O ₀ –I/O ₇		26 17	39 25	ns	C _L = 45 pF, R _L = 667 Ω
t _{PHL}	Propagation Delay, Clear to I/O ₀ –I/O ₇		26	40	ns	
t _{PZH} t _{PZL}	Output Enable Time		13 19	21 30	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		10 10	15 15	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _W	Clock Pulse Width HIGH	25			ns	V _{CC} = 5.0 V
t _W	Clock Pulse Width LOW	13			ns	
t _W	Clear Pulse Width LOW	20			ns	
t _S	Data Setup Time	20			ns	
t _S	Select Setup Time	35			ns	
t _H	Data Hold Time	0			ns	
t _H	Select Hold Time	10			ns	
t _{rec}	Recovery Time	20			ns	

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3-STATE WAVEFORMS

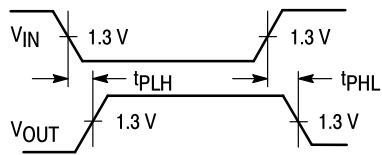


Figure 1

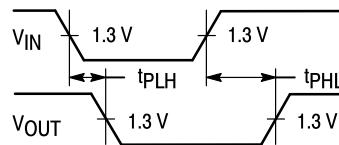


Figure 2

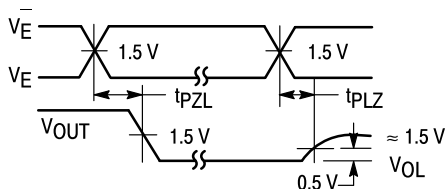


Figure 3

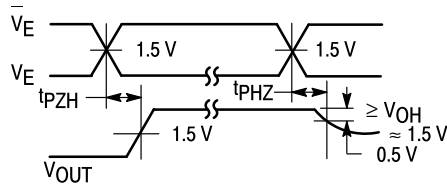
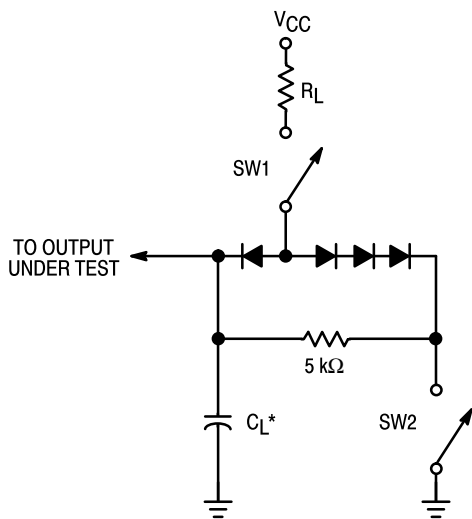


Figure 4

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PLZ}	Closed	Closed
t _{PHZ}	Closed	Closed

Figure 5

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SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed



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