

TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699 SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

D2424, JANUARY 1981

- 4-Bit Counters/Registers
- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- 'LS696 . . . Decade Counter, Direct Clear
- 'LS697 . . . Binary Counter, Direct Clear
- 'LS698 . . . Decade Counter, Synchronous Clear
- 'LS699 . . . Binary Counter, Synchronous Clear

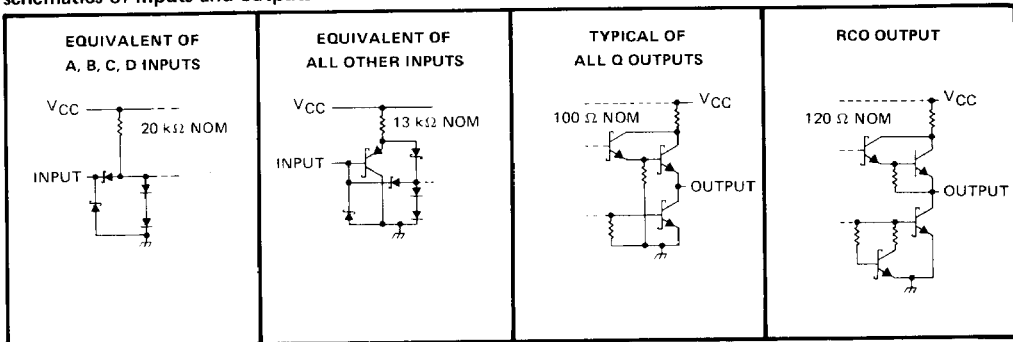
description

These low-power Schottky LSI devices incorporate synchronous up/down counters, four-bit D-type registers, and quadruple two-line to one-line multiplexers with three state outputs in a single 20-pin package. The up/down counters are programmable from the data inputs and feature enable P and enable \bar{T} and a ripple-carry output for easy expansion. The register/counter select input R/C, selects the counter when low and the register when high for the three-state outputs, Q_A, Q_B, Q_C, and Q_D. These outputs are rated at 12 and 24 milliamperes (54LS/74LS) for good bus driving performance.

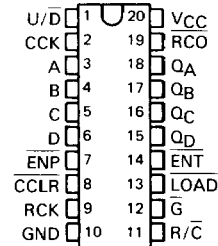
Both the counter clock CCK and register clock RCK are positive-edge triggered. The counter clear CCLR is active low and is a synchronous on the 'LS696 and 'LS697, synchronous on the 'LS698 and 'LS699. Loading of the counter is accomplished when \overline{LOAD} is taken low and a positive transition occurs on the counter clock CCK.

Expansion is easily accomplished by connecting \overline{RCO} of the first stage to \overline{ENT} of the second stage, etc. All ENP inputs can be tied common and used as a master enable or disable control.

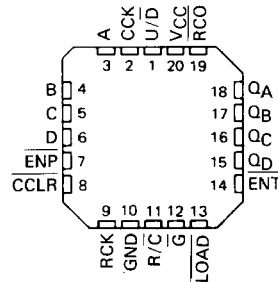
schematics of inputs and outputs



SN54LS696 THRU SN54LS699 . . . J PACKAGE
SN74LS696 THRU SN74LS699 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS696 THRU SN54LS699 . . . FK PACKAGE
SN74LS696 THRU SN74LS699 . . . FN PACKAGE
(TOP VIEW)



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PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

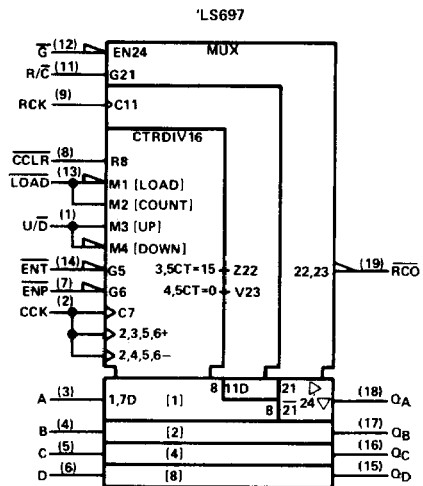
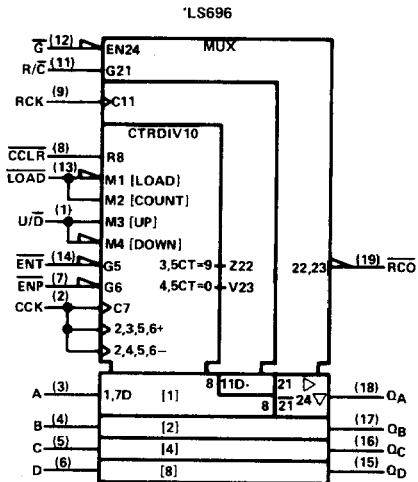
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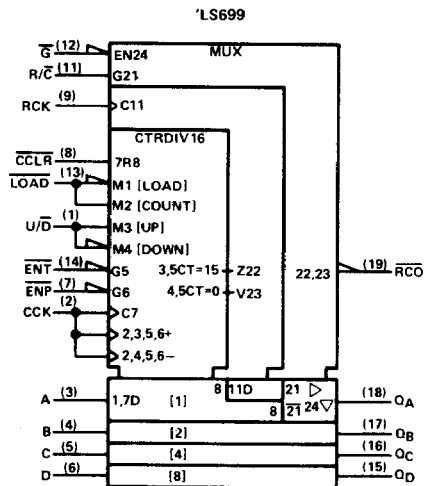
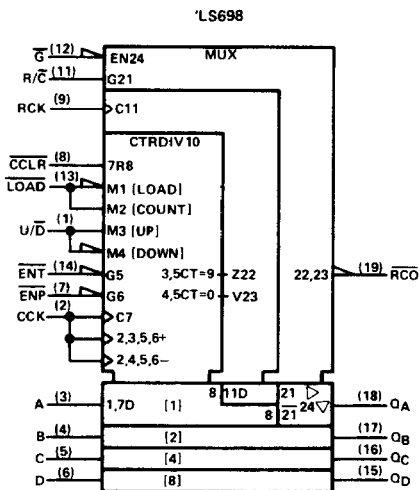
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logic symbols



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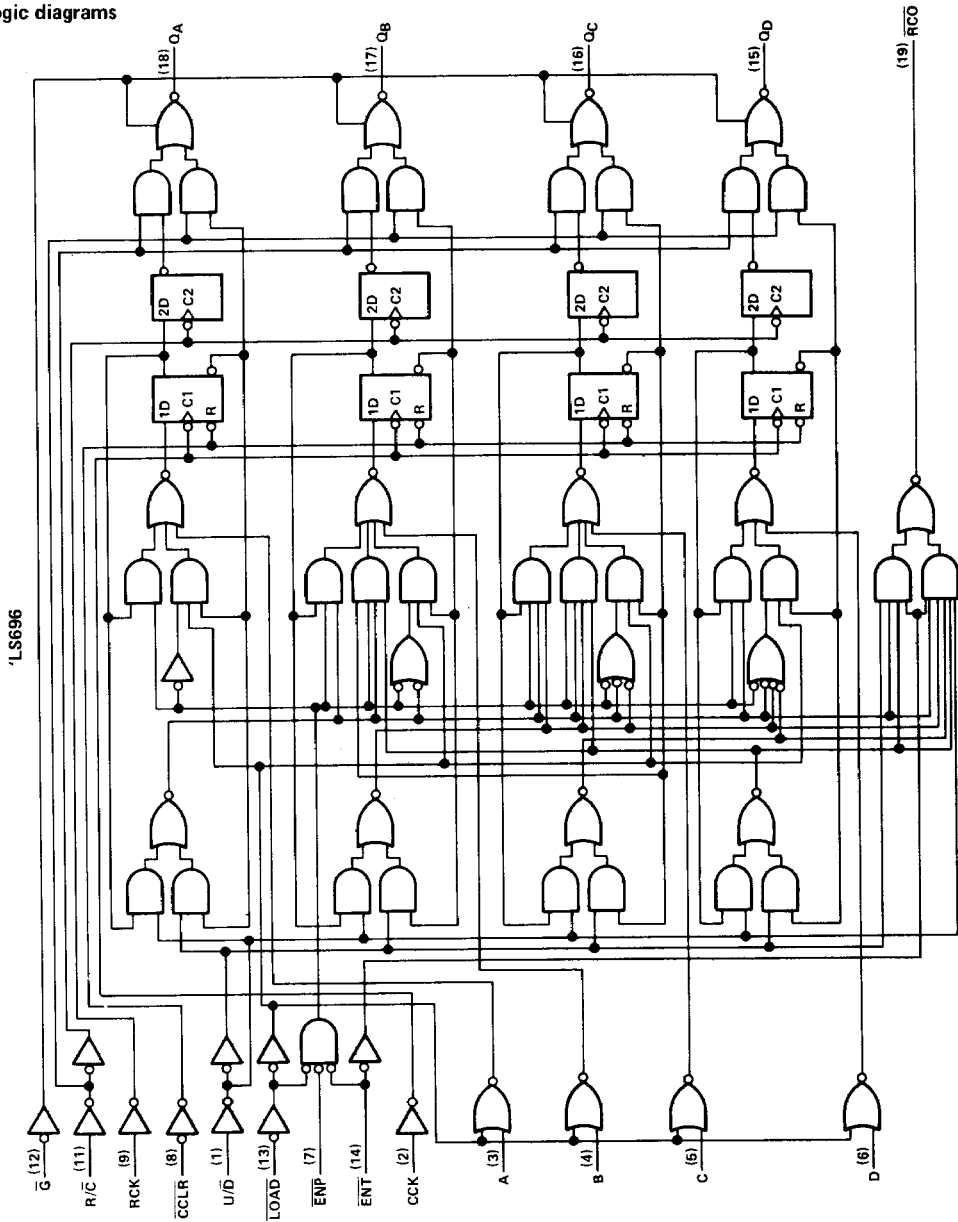
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Pin numbers shown on logic notation are for DW, J or N packages.

TYPES SN54LS696, SN74LS696
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams



Pin numbers shown on logic notation are for DW, J or N packages.

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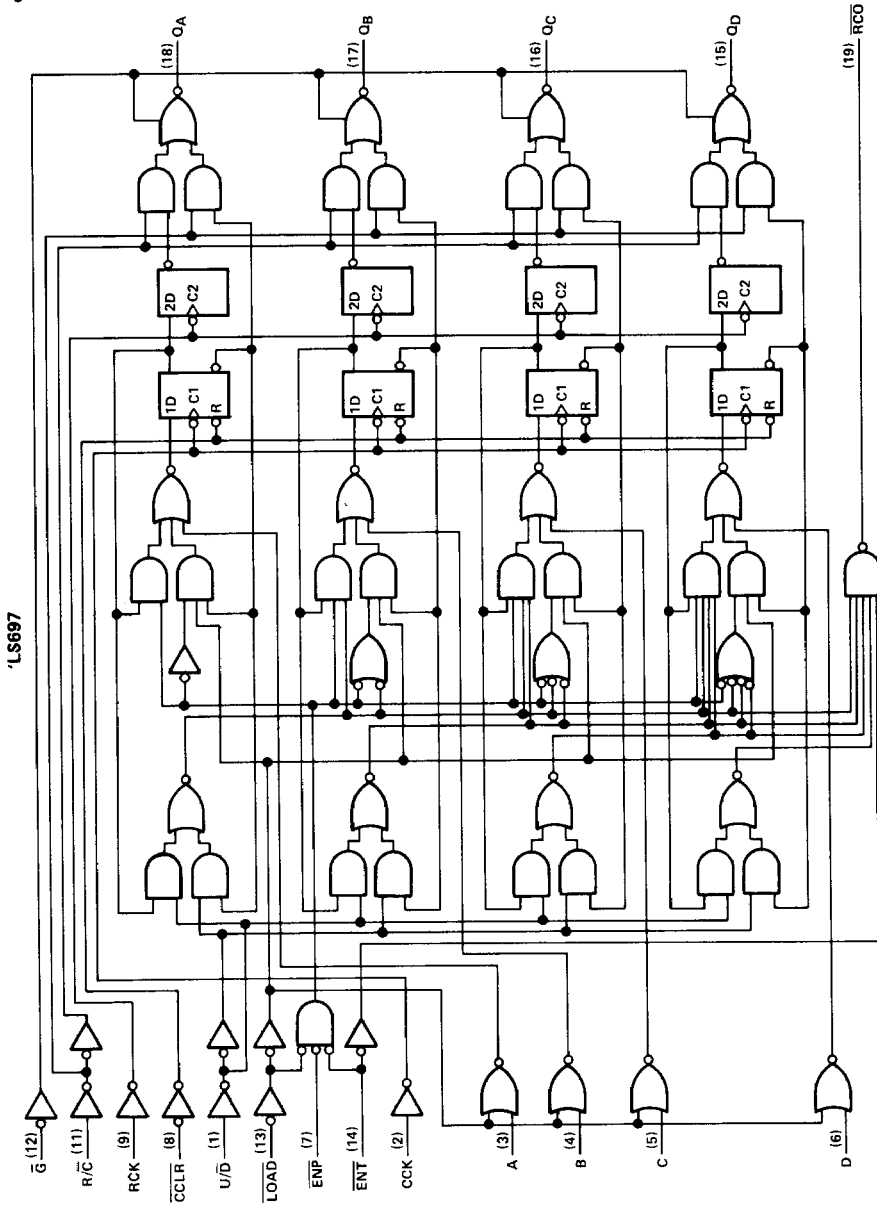


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TYPES SN54LS697, SN74LS697
SYNCHRONOUS UP/DOWN COUNTERS
WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (continued)

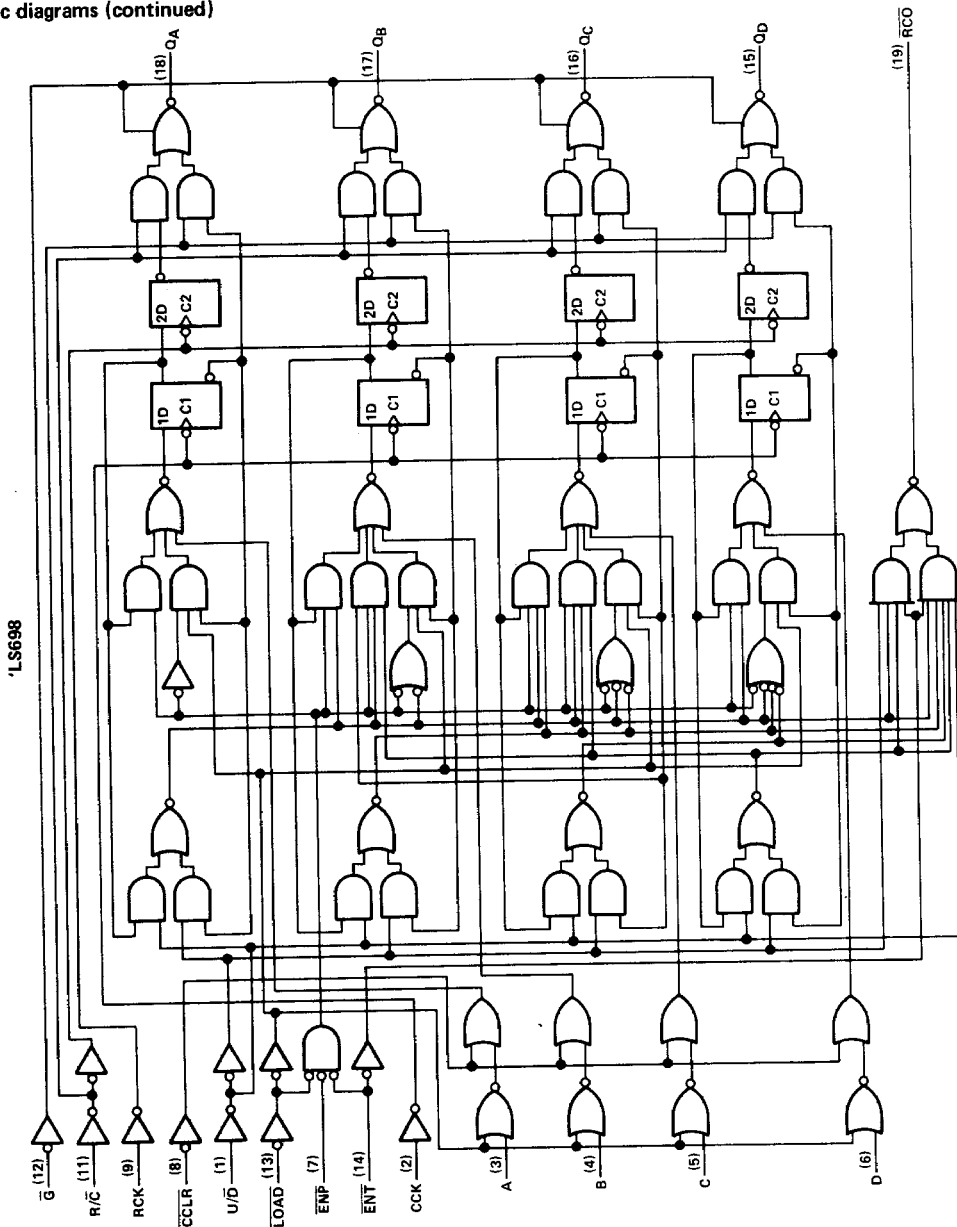


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TYPES SN54LS696, SN74LS696, SN54LS698, SN74LS698
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

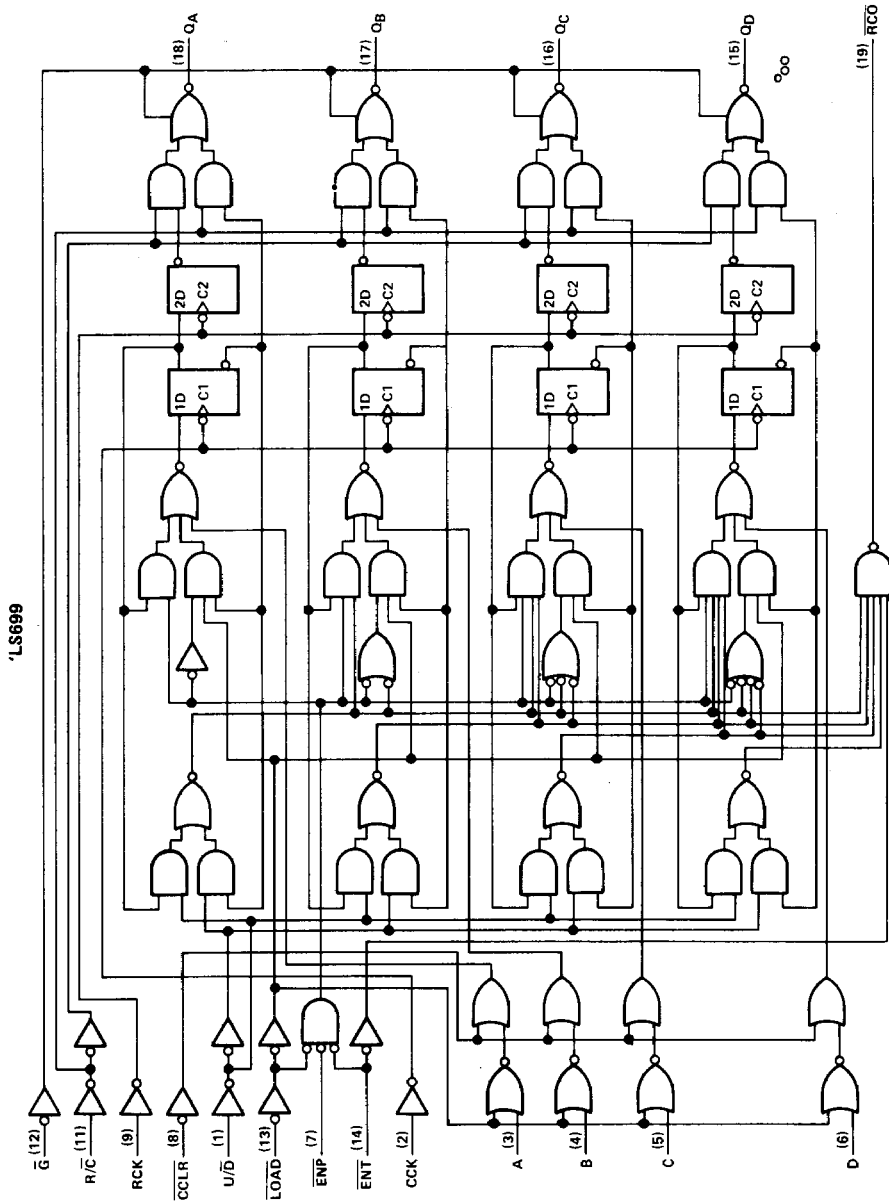
logic diagrams (continued)



Pin numbers shown on logic notation are for DW, J or N packages.

TYPES SN54LS697, SN74LS697, SN54LS699, SN74LS699
SYNCHRONOUS UP/DOWN COUNTERS
WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

logic diagrams (continued)



Pin numbers shown on logic notation are for DW, J or N packages.

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TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699 SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS696 thru SN54LS699	-55°C to 125°C
SN74LS696 thru SN74LS699	0°C to 70°C
Storage temperature range	- 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
I_{OH}	High-level output current	Q			- 1			mA	
		RCO			- 0.4				
I_{OL}	Low-level output current	Q			12			mA	
		RCO			4				
f_{clock}	Clock frequency	CCK		0	20	0	20	MHz	
		RCK		0	20	0	20		
t_w	Pulse duration	CCK high or low			25			ns	
		RCK high or low			25				
		'LS696, 'LS697 CCLR low			20				
t_{su}	Setup time before CCK ↑	A thru D			30			ns	
		ENP or ENT			30				
		LOAD			30				
		U/D			35				
		'LS696, 'LS697, CCLR inactive			25				
		'LS698, 'LS699, CCLR			30				
t_{su}	Setup time CCK ↑ before RCK ↑ (see Note 2)	30			30			ns	
t_h	Hold time	0			0			ns	
T_A	Operating free-air temperature	- 55		125		0		70	°C

NOTE 2: This set up time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

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TYPES SN54LS696 THRU SN54LS699, SN74LS696 THRU SN74LS699 SYNCHRONOUS UP/DOWN COUNTERS WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH} High-level input voltage		2			2			V	
V _{IL} Low-level input voltage				0.7			0.8	V	
V _{IK} Input clamp voltage	V _{CC} =MIN, I _I =-18 mA			-1.5			-1.5	V	
V _{OH} High-level output voltage	Any Q	V _{CC} =MIN, V _{IH} =2 V, V _{IL} =V _{IL} max	I _{OH} =-1 mA	2.4	3.1			V	
	Any Q		I _{OH} =-2.6 mA			2.4	3.1		
	RCO		I _{OH} =-400 μA	2.5	3.2	2.7	3.2		
V _{OL} Low-level output voltage	Any Q	V _{CC} =MIN, V _{IH} =2 V, V _{IL} =V _{IL} max	I _{OL} =12 mA			0.25	0.4	V	
	Any Q		I _{OL} =24 mA			0.35	0.5		
	RCO		I _{OL} =4 mA		0.25	0.4	0.25		0.4
	RCO		I _{OL} =8 mA			0.35	0.5		
I _{OZH} Off-state output current, high-level voltage applied	Any Q	V _{CC} =MAX, \bar{G} at 2 V, V _O =2.7 V				20	20	μA	
I _{OZL} Off-state output current, low-level voltage applied	Any Q	V _{CC} =MAX, \bar{G} at 2 V, V _O =0.4 V				-20	-20	μA	
I _I Input current at maximum input voltage		V _{CC} =MAX, V _I =7 V			0.1		0.1	mA	
I _{IH} High-level input current		V _{CC} =MAX, V _I =2.7 V			20		20	μA	
I _{IL} Low-level input current	A thru D	V _{CC} =MAX, V _I =0.4 V				-0.4	-0.4	mA	
	All others					-0.2	-0.2		
I _{OS} Short-circuit output current §	Any Q	V _{CC} =MAX, V _O =0 V		-30	-130	-30	-130	mA	
	RCO			-20	-100	-20	-100		
I _{CC} H Supply current, outputs high		V _{CC} =MAX,	See Note 3	46	65	46	65	mA	
I _{CC} L Supply current, outputs low		All outputs open	See Note 4	48	70	48	70		
I _{CC} Z Supply current, outputs off			See Note 5	48	70	48	70		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 3. I_{CC}H is measured after two 4.5 V to 0 V to 4.5 V pulses have been applied to CCK and RCK while \bar{G} is grounded and all other inputs are at 4.5 V.

4. I_{CC}L is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while all other inputs are grounded.

5. I_{CC}Z is measured after two 0 V to 4.5 V to 0 V pulses have been applied to CCK and RCK while \bar{G} is at 4.5 V and all other inputs are grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS696, 'LS697			'LS698, 'LS699			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	CCK↑	RCO	R _L = 2 kΩ, C _L = 15 pF	23	40		23	40	ns	
t _{PHL}				23	40		23	40	ns	
t _{PLH}				13	20		13	20	ns	
t _{PHL}	ENT	RCO		13	20		13	20	ns	
t _{PLH}				12	20		12	20	ns	
t _{PHL}				17	25		17	25	ns	
t _{PLH}	CCK↓	Q	12	20		12	20	ns		
t _{PHL}			17	25		17	25	ns		
t _{PLH}			12	20		12	20	ns		
t _{PHL}	RCK↑	Q	17	25		17	25	ns		
t _{PLH}			23	40				ns		
t _{PHL}			16	25		16	25	ns		
t _{PLH}	CCLR↓	Q	16	25		16	25	ns		
t _{PHL}			16	25		16	25	ns		
t _{PLH}			19	30		19	30	ns		
t _{PZH}	\bar{G} ↓	Q	19	30		19	30	ns		
t _{PZL}			17	30		17	30	ns		
t _{PHZ}			17	30		17	30	ns		
t _{PLZ}	\bar{G} ↑	Q	17	30		17	30	ns		
t _{PLZ}			17	30		17	30	ns		

NOTE 6: See General Information Section for load circuits and voltage waveforms.

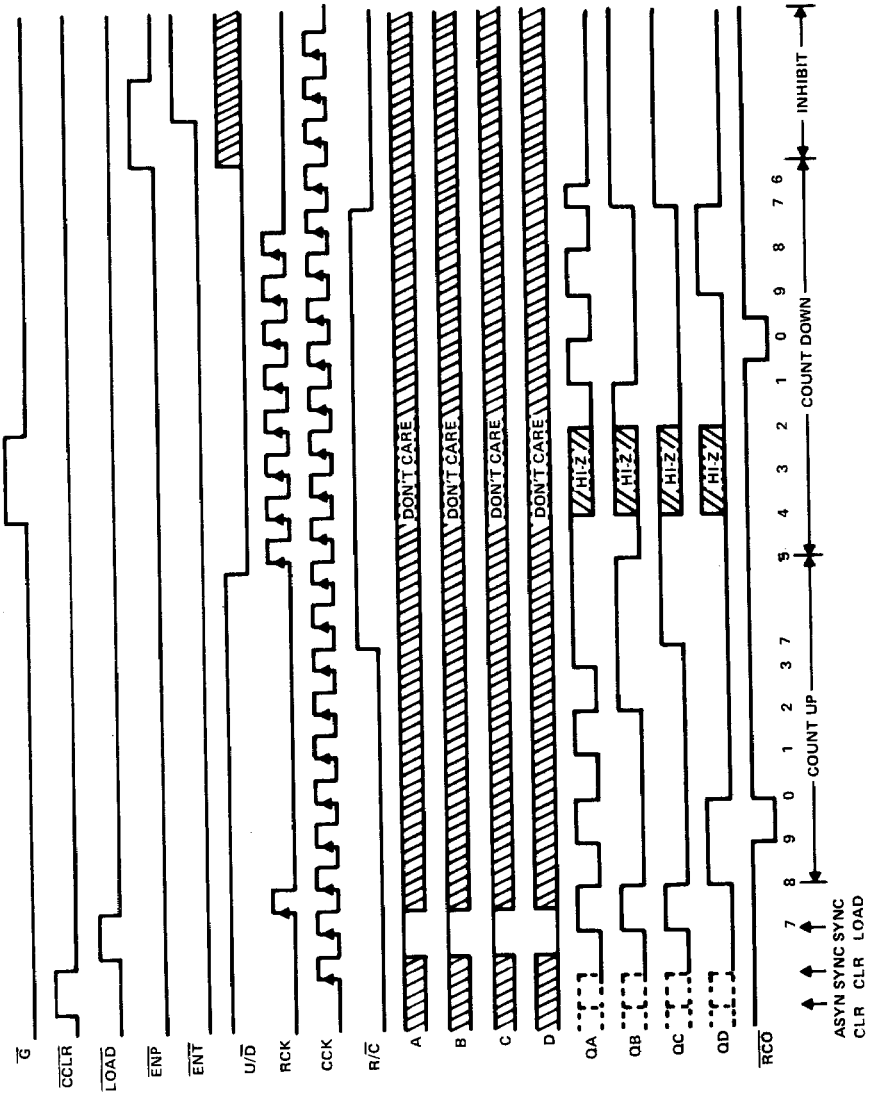
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TTL DEVICES

TYPES SN54LS696, SN54LS698, SN74LS696, SN74LS698
 SYNCHRONOUS UP/DOWN COUNTERS
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typical operating sequences

'LS696 DECADE COUNTER, Asynchronous Clear
 'LS698 DECADE COUNTER, Synchronous Clear



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TYPES SN54LS697, SN54LS699, SN74LS697, SN74LS699
 SYNCHRONOUS UP/DOWN COUNTERS
 WITH OUTPUT REGISTERS AND MULTIPLEXED 3-STATE OUTPUTS

typical operating sequences (continued)

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TTL DEVICES

'LS697 BINARY COUNTER, Asynchronous Clear
 'LS699 BINARY COUNTER, Synchronous Clear

